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PROGRAMMABLE ACOUSTIC SIGNAL PROCESSING DEVICES

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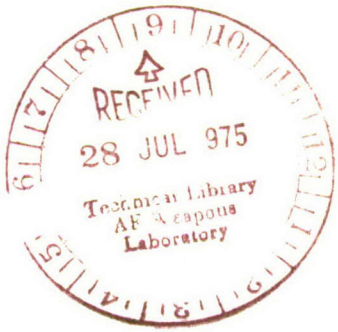

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20. ABSTRACT *(Continue on reverse side if necessary and identify by block number)*

The main objectives of this program were:

1. To develop advanced programmable signal processing devices which employ surface acoustic wave tapped delay lines and integrated control circuits. This included the design, fabrication, and evaluation of electronically programmable tapped delay line (PTDL) waveform generators and matched filters with ≥ 100 taps for spread spectrum system applications at 435 MHz with ~ 20 MHz chip rates.

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20. Abstract (Cont)

2. To design a transceiver which utilizes the PTDL's developed in Task 1 above as matched filters and demonstrate signal transmission and electronically programmed decoding of spread spectrum phase coded waveforms at 435 MHz with 20 MHz chip rates.

3. To deliver six 435 MHz PTDL's to ECOM together with two demonstration exerciser boxes and the transceiver.

These objectives were met after the special problems associated with 435 MHz operation were identified and analyzed.

The acoustic and microelectronic design details and initial predicted PTDL performance are given in Section 2. Section 3 contains details of the experimental results and the loaded transmission line effects experienced at 435 MHz which had to be analyzed in detail before good agreement between theory and experiment could be achieved.

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ABSTRACT

The main objectives of this program were:

1. To develop advanced programmable signal processing devices which employ surface acoustic wave tapped delay lines and integrated control circuits. This included the design, fabrication, and evaluation of electronically programmable tapped delay line (PTDL) waveform generators and matched filters with ≥100 taps for spread spectrum system applications at 435 MHz with ~20 MHz chip rates.

2. To design a transceiver which utilizes the PTDL's developed in task 1 above as matched filters and demonstrate signal transmission and electronically programmed decoding of spread spectrum phase coded waveforms at 435 MHz with 20 MHz chip rates.

3. To deliver six 435 MHz PTDL's to ECOM packaged as part of two demonstration exerciser boxes and the transceiver (i.e. two PTDL's per package).

These objectives were met after the special problems associated with 435 MHz operation were identified and analyzed.

The acoustic and microelectronic design details and initial predicted PTDL performance are given in Section 2. Section 3 contains details of the PTDL experimental results and a discussion of the loaded transmission line effects experienced at 435 MHz which were analyzed in detail in order to achieve agreement between theory and experiment.

CONCLUSIONS

The results of this program demonstrate that electronically programmed matched filters for decoding spread spectrum phase coded waveforms at 435 MHz with 20 MHz chip rates are feasible and good UHF transceiver performance can be achieved with these devices. The UHF matched filter electrical performance achieved on this contract (dynamic range and peak/sidelobe ratios) are not as good as the excellent

results achieved at VHF frequencies and lower chip rates (70 MHz and 10 MHz respectively) on other programs. However, the steps necessary to significantly improve performance at 435 MHz have been identified and could be implemented in a new design.

The silicon on sapphire CMOS integrated control circuit fabrication represented the major effort on this program. The CMOS/SOS semi-selfaligned silicon nitride gate process used for this circuit was a relatively new technology at the start of this program and its successful implementation took somewhat longer than anticipated. These fabrication problems were essentially solved in late 1974, currently yields on this particular CMOS/SOS are ~20 percent and would probably be as high as 50 percent in volume production.

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1. INTRODUCTION

One major objective of this program has been to develop advanced programmable signal processing devices which employ surface wave tapped delay lines and integrated control circuits. The effort includes the design, fabrication and evaluation of an electronically programmable sequence generator and matched filter. Performance goals are as follows:

Frequency of Operation	435 MHz
Number of Taps (Chips)	100 Minimum
Chip Rate (Bandwidth)	~20 MHz
Correlation Peak to Sidelobe Ratio	Within 1 dB of Theoretical for any given code over the temperature range
Coding	Pseudorandom Biphase
Data Loading Time	10 μsec
Operating Temperature Range	0 to 50 deg C

The design approach selected for implementation on this effort consists of a surface acoustic wave ST cut quartz tapped delay line combined with CMOS on sapphire integrated control circuits.

Another major task has been the design, fabrication and evaluation of a 435 MHz transceiver using these programmable tapped delay lines as matched filters in the receiver. The transceiver specifications are as follows:

Transmitter

Power Output	2 watt (CW), 3 watt (saturation)
Carrier Frequency	435 MHz
Data Rate	Selectable 19.2, 4.8, 2.4, 1.2 Kbps
Modulation	Differentially encoded and then P.N. spread at a 20.7 MHz chip rate. The output is then biphase modulated.
Tx Duty Cycle	Burst Mode = 6.5 percent Continuous Mode = 100 percent
Code Length (Selectable)	Long = 8,388,480 chips Short = 7,616 chips
Power Supply Requirement	+28v DC ±5 percent

Receiver

Sensitivity	-100 dBm at 16 dB Eb/No
N. F. (Front End)	6 dB Maximum
Surface Acoustic Wave Device Used	(2) 435 MHz = f_c, programmable at 20.7 MHz chip rate
Provides Synch Lock Indication - Acquisition is within following Limits:	Short (burst mode) = 5.83 ms Long (burst mode) = 6.42 sec Short (continuous mode) = 360 μsec Long (continuous mode) = .4 sec
Power Supply Requirement	+28v DC ±5 percent

Section 2 summarizes the acoustic and microelectronic designs and contains overall programmable tapped delay line performance predictions based on a model which was known to be accurate at low frequencies (≤120 MHz). Also included in Section 2 is an analysis of several of the major factors which determine whether an active or passive waveform generation technique should be used for a specific spread spectrum system.

Experimental techniques and results are described in Section 3. Processing problems and solutions are described. Significant discrepancy between actual PTDL performance and initial design predictions of Section 2 was noted in terms of both the insertion loss to a single tap and the shape of the impulse response. However, a revised model which considered the signal sum lines in the integrated circuits as a loaded transmission line removed most of the discrepancy. Section 3.5 describes this model and compares theory and experiment.

Section 4 outlines the transceiver design and includes experimental results while Section 5 contains the conclusions drawn on the basis of the work performed on this contract and recommendations for additional work.

2. DESIGN OF 435 MHz PTDL

2.1 INTRODUCTION

The basic design and performance predictions for both the surface acoustic wave tapped delay line (TDL) and the silicon on sapphire integrated control circuit (STDL) were described in the interim report. Only a brief summary of that data will be given in this section together with the results of additional analysis performed since the interim report.

The acoustic TDL is first considered separately and then with a lumped element circuit consisting of the semiconductor diode switches and isolating biasing resistors. Performance predictions of insertion loss and autocorrelation function are given in Section 2.4.

Spread spectrum waveform generation can be active or passive. Section 2.5 analyzes some problems of active waveform generation and provides some further information on which an active vs passive waveform generation decision is made.

2.2 ACOUSTIC TAPPED DELAY LINE

The factors affecting tapped delay line performance were discussed in detail in the interim report and the final design outlined. The input transducer consists of 21 quarter wavelength finger pairs with 150 wavelengths in the aperture while the tap array contains 128 single finger pair taps with $3\lambda/8$ finger widths and gaps. The tap array is apodized 2:1 in overlap from the first to last tap so the tap nearest the input transducer (first tap) has a 75λ aperture while the last tap (128th tap) has a 150λ aperture. The apodization was selected on the basis of experimental results described in the interim report.

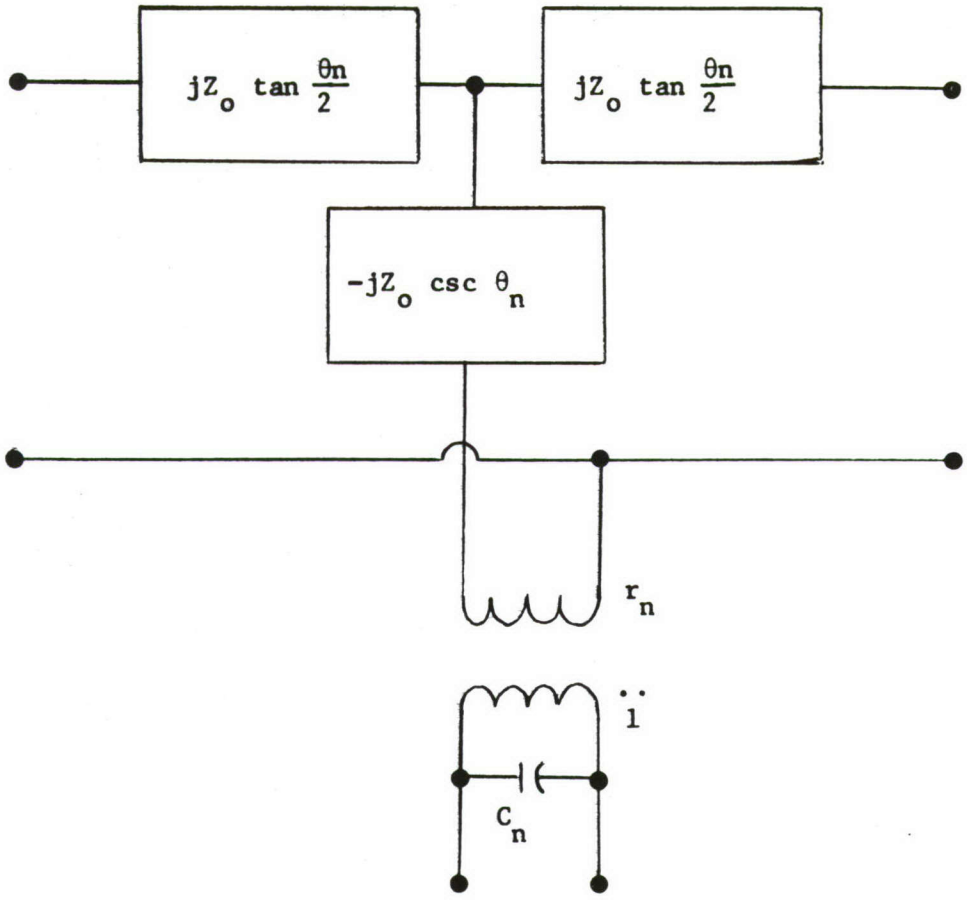
A conventional equivalent circuit approach was used to analyze the performance of this acoustic tapped delay line. In this approach the surface acoustic wave IDT is treated as an transmission line using the crossed-field equivalent circuit of Figure 1(a). Each section of the IDT which includes one electrode and two half-gaps on each side as seen in Figure 1(b) is modeled by one equivalent circuit. In the model θ is the transit angle across each section and is given by

$$\theta = \pi f/f_o$$

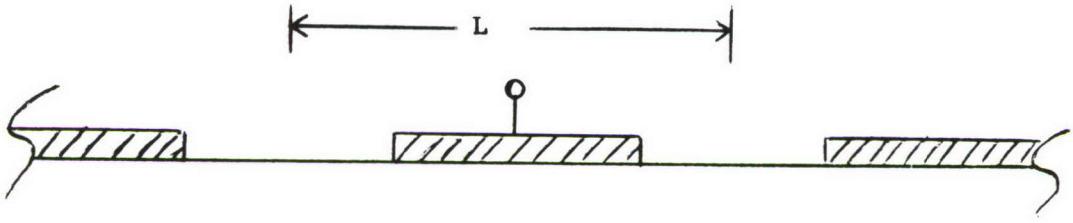
where f_o is the synchronous frequency defined by $f_o = V/2L$ where L is one-half the electrode periodicity and V is the acoustic velocity. The transformer provides for the electroacoustic interaction between the acoustic and electrical generator or loading circuits and has a turns ratio for the nth electrode given by

$$r_n = \pm \sqrt{2f_o C_n k^2 Z_o}$$

The sign is chosen to correspond to a + or - electrode.



(a) Equivalent Circuit of Single Electrode Restion



(b) Electrodes and Transmission Line of Length L

Figure 1. IDT Modeling

C_n is the static capacitance of the nth electrode, k^2 the electromechanical coupling coefficient and Z_o is the acoustic wave impedance. Each circuit is a 3-port with two acoustic ports and one electrical port. Thus the circuit can be represented by a symmetric 3 x 3 admittance matrix $y_{ij}^{(n)}$ where each element of the matrix is given by

$$y_{11}^{(n)} = y_{22}^{(n)} = -j \cot \theta$$

$$y_{12}^{(n)} = j \csc \theta$$

$$y_{13}^{(n)} = y_{23}^{(n)} = -jr_n \tan \theta/2$$

$$y_{33}^{(n)} = j[\omega C_n + 2r_n^2 \tan \theta/2]$$

It can be shown that no generality is lost by letting $Z_o = 1$.

With each electrode section modeled by the circuit of Figure 1(a) and the admittance matrix above the complete transducer is constructed by cascading many such circuits together as in Figure 2. Adjacent acoustic ports are connected in series and all the electrical ports are connected in parallel. This procedure yields a total 3 x 3 admittance matrix which represents the whole transducer. The total matrix is calculated from the recursion relations for n = 2, 3, ..., N

$$Y_{11}^{(n)} = y_{11}^{(n)} - \frac{y_{12}^{(n)2}}{D^{(n)}}$$

$$Y_{12}^{(n)} = -\frac{y_{12}^{(n)} Y_{12}^{(n-1)}}{D^{(n)}}$$

$$Y_{22}^{(n)} = Y_{22}^{(n-1)} - \frac{Y_{12}^{(n-1)2}}{D^{(n)}}$$

$$Y_{13}^{(n)} = y_{13}^{(n)} - \frac{y_{12}^{(n)} y^{(n)}}{D^{(n)}}$$

$$Y_{23}^{(n)} = Y_{23}^{(n-1)} - \frac{Y_{12}^{(n-1)} y^{(n)}}{D^{(n)}}$$

$$Y_{33}^{(n)} = Y_{33}^{(n-1)} + y_{33}^{(n)} - \frac{y^{(n)2}}{D^{(n)}}$$

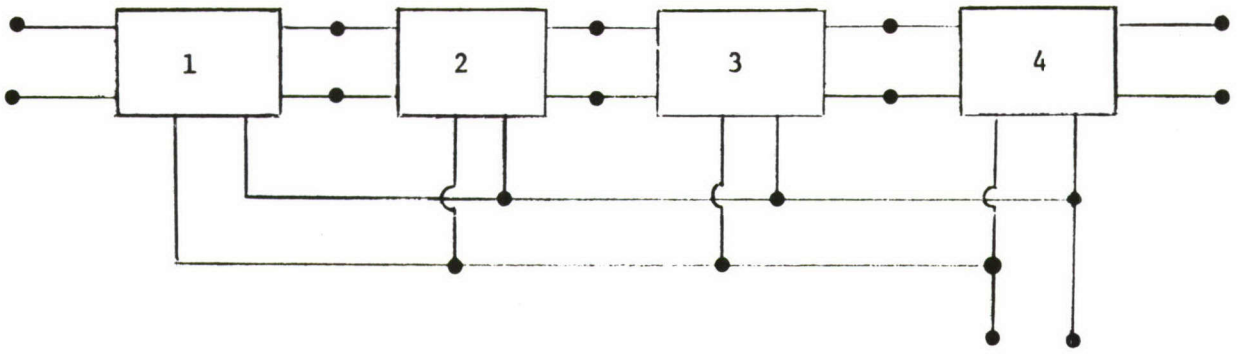


Figure 2. Schematic of Cascading of Circuit Models.
Acoustic Ports in Series and Electrical Ports in Parallel

where N is the total number of electrodes and

$$Y_{ij}^{(1)} = y_{ij}^{(1)},$$

$$D^{(n)} = y_{22}^{(n)} + Y_{11}^{(n-1)}$$

$$y^{(n)} = y_{23}^{(n)} + Y_{13}^{(n-1)} \quad .$$

Thus $Y_{ij}^{(N)}$ are the coefficients of the total admittance matrix. A computer program incorporating the above model was used to evaluate the acoustic design. The program takes into account any required apodization and tap phase coding and output matching network parameters in addition to providing the complete frequency domain transfer function over an arbitrary frequency range. A discrete Fourier transform analysis is also carried out to obtain the time domain (autocorrelation) performance.

The time domain performance predictions for the subject 435 MHz TDL is shown in Figure 3 which is seen to predict a peak to maximum sidelobe ratio of 22.34 dB for the 127 chip PN code selected for analysis. An expansion of the main correlation peak is shown in Figure 4 which indicates that regeneration effects discussed in the interim report have been reduced to negligible levels by the appropriate design precautions.

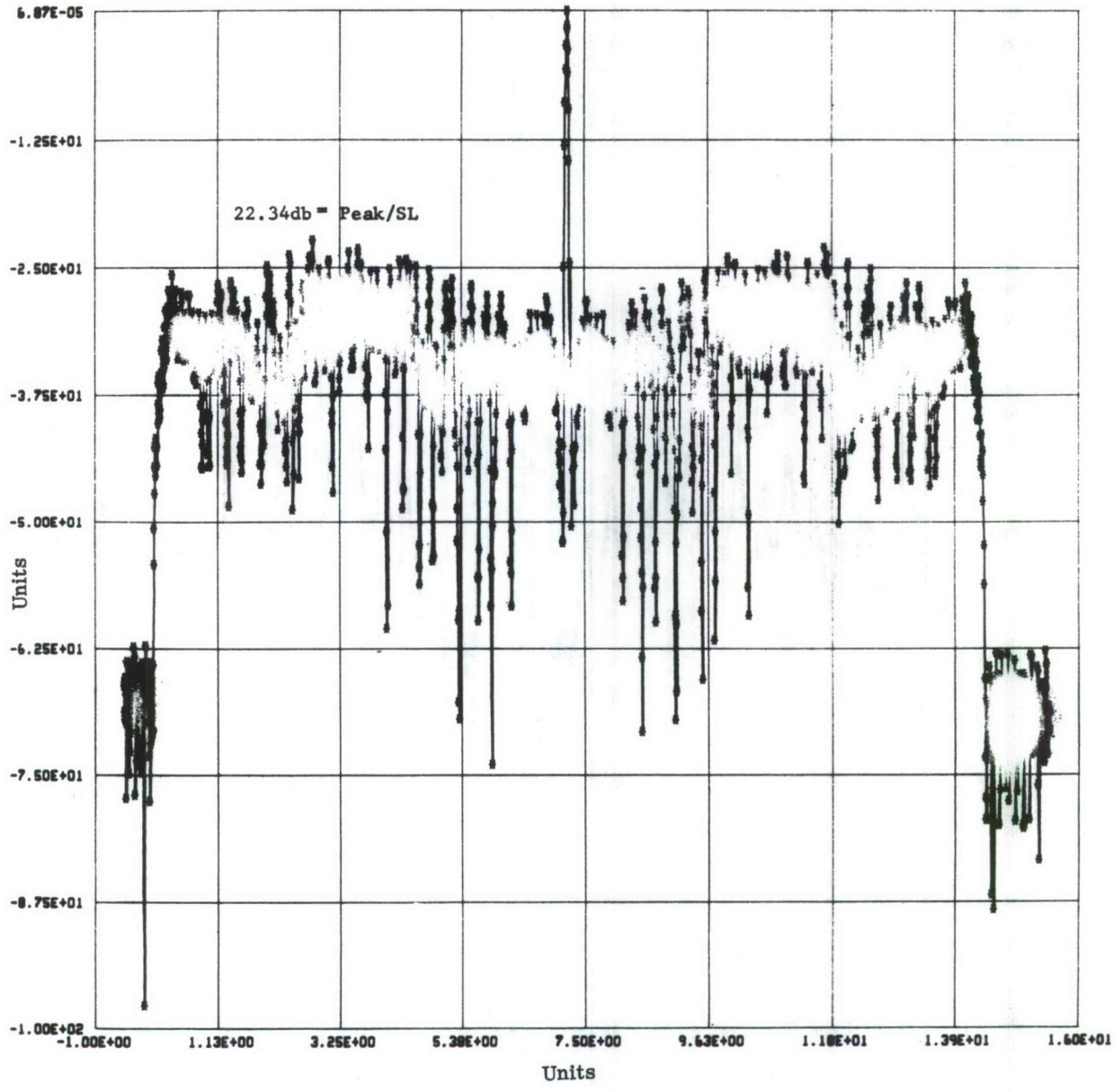


Figure 3. Time Domain Performance of 127 Chip PN Coded Tapped Delay Line at 435 MHz

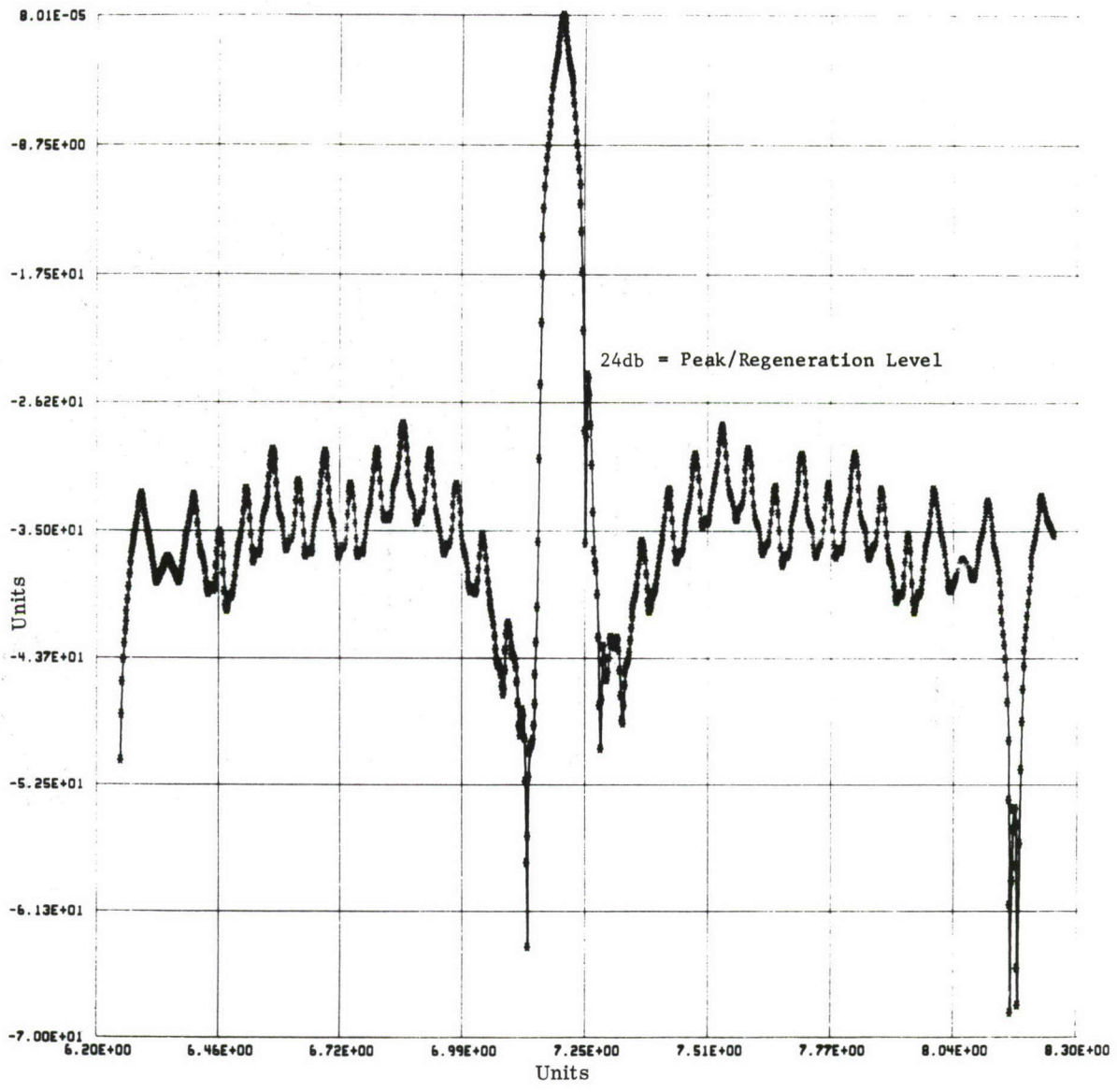


Figure 4. Expanded Correlation Peak of Figure 3

Insertion loss to the first tap was predicted to be 72 dB. This is in good agreement with the 68 dB predicted in the interim report for a full aperture tap using a simpler mouel since the half-aperture apodization of the first tap would be expected to increase insertion loss by 6 dB over a full aperture tap.

2.3 MICROELECTRONIC INTEGRATED CONTROL CIRCUIT

The task which required the major effort on this program was the design and fabrication of the silicon-on-sapphire integrated microcircuit used for switching the acoustic taps. A completely new design was required using CMOS/SOS since the previously proven PMOS/SOS circuit approach would not meet the speed requirements of this contract. The dual diode bridge switching circuit, which was successfully used and characterized on a previous PMOS integrated control circuit (Contract F33615-72-C-1169) is still used, however.

The switching microcircuit used for the programmable surface acoustic wave delay line is blocked out in Figure 5. It is composed of a static 16 bit serial in, serial/parallel out data register, a 16 bit parallel in, parallel out storage register, and 16 single pole, double-throw diode bridge switches and switch drivers. Silicon-on-sapphire was selected as the fabrication technology as it permits construction of the very low capacitance diode switches required for tap switching at 435 MHz. Earlier designs for the circuit utilized PMOS transistors to implement the shift registers but the maximum operating speed attainable was only 10 MHz and not sufficient for this project. Since a goal on this program was to achieve a maximum code loading time of 10 μsec for 128 bits, the clock rate for serial data input had to be in excess of $128/10^{-5}$ or 12.8 MHz. A CMOS on sapphire approach was selected which

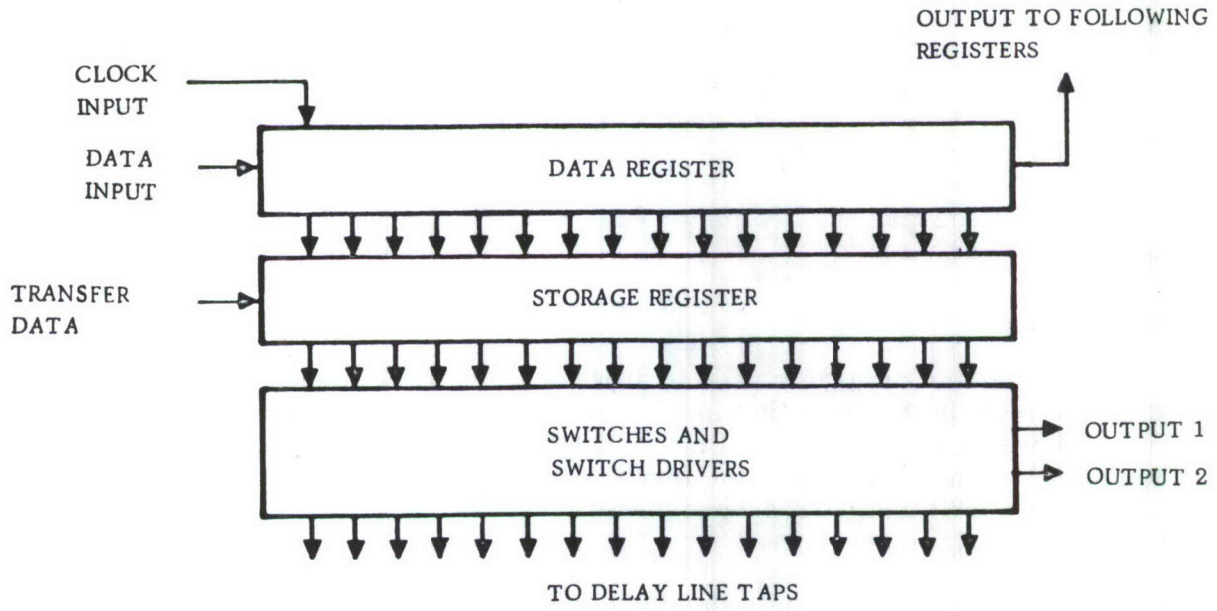


Figure 5. Tap Switching Circuit Diagram

used a semi-self-aligning gate technique to reduce gate to drain overlap with consequent parasitic capacitance reduction and speed increase. Use of CMOS circuits, in addition to allowing high speed operation, permits simplification of the control circuits, reduction of the number of power supplies required to one, a single 10 to 12V supply, and major reduction in the static power requirements.

A computer simulation of a CMOS shift register circuit, utilizing the proposed design rules was performed before the photomasks were fabricated to determine what upper limit on clocking frequency could be expected. This simulation, described earlier in the interim report for this program, indicated that the upper limit of clocking frequencies would be in the order of 47 MHz when operated at a +10 volts power supply level.

Figure 6 is a photograph of the microcircuit developed for this program. If an imaginary horizontal line is drawn between the top of the two metal pads labeled "T", the 16 bit data register will be located above it, the 16 bit storage register will be located below it and the switch driving transistors will be found between the two pads labeled "Gnd". Extending below the "Gnd" pads are 32 metal buses used to physically separate the digital circuitry from the RF switching located below and adjacent to the two sum lines $\sum_1$ and $\sum_2$. The delay line taps are connected to pads numbered 1 through 16.

Organization of the die is such that 16 cells, 100 mils x 4.5 mils, are stepped horizontally across the die. Each cell contains all circuitry, illustrated in Figure 7, necessary for the control of one tap.

Each triangle represents a CMOS inverter composed of one NMOS and one PMOS transistor as illustrated in Figure 8.

Each rectangle is a transmission gate also containing one NMOS and one PMOS transistor as illustrated in Figure 9(a) and (b).

Inverters I_1 through I_4 and transmission gates T_1 through T_4 form a master/slave type D flip-flop where data present at the input appears at the output at the trailing edge of the clock. The two cross-connected NOR gates form a latch storage circuit which accepts data from the data register when the transfer gates, T_5 and T_6 are operated. The triangles labeled BI are CMOS buffer/inverters used to drive the diode bridge switches.

2.4 ACOUSTIC/MICROELECTRONIC INTERFACE (ANALYSIS)

The computer programs used to analyze the acoustic tapped delay line were modified to include the acoustic tap switching circuits. The overall model and the diode switches were as shown in Figures 10, 11, and 12. The diodes were considered as lumped element resistors in the forward direction and lossless capacitors under reverse bias conditions. Cross-overs were modeled as dissipative capacitors (R_c and C_c).

The program was run with the diode target parameters of 100 ohm forward resistance and .05 pf reverse bias capacitance. Diode bias resistors of 20 KΩ value were assumed together with cross-overs of R_c = 100 ohms and C_c = .02 pf.

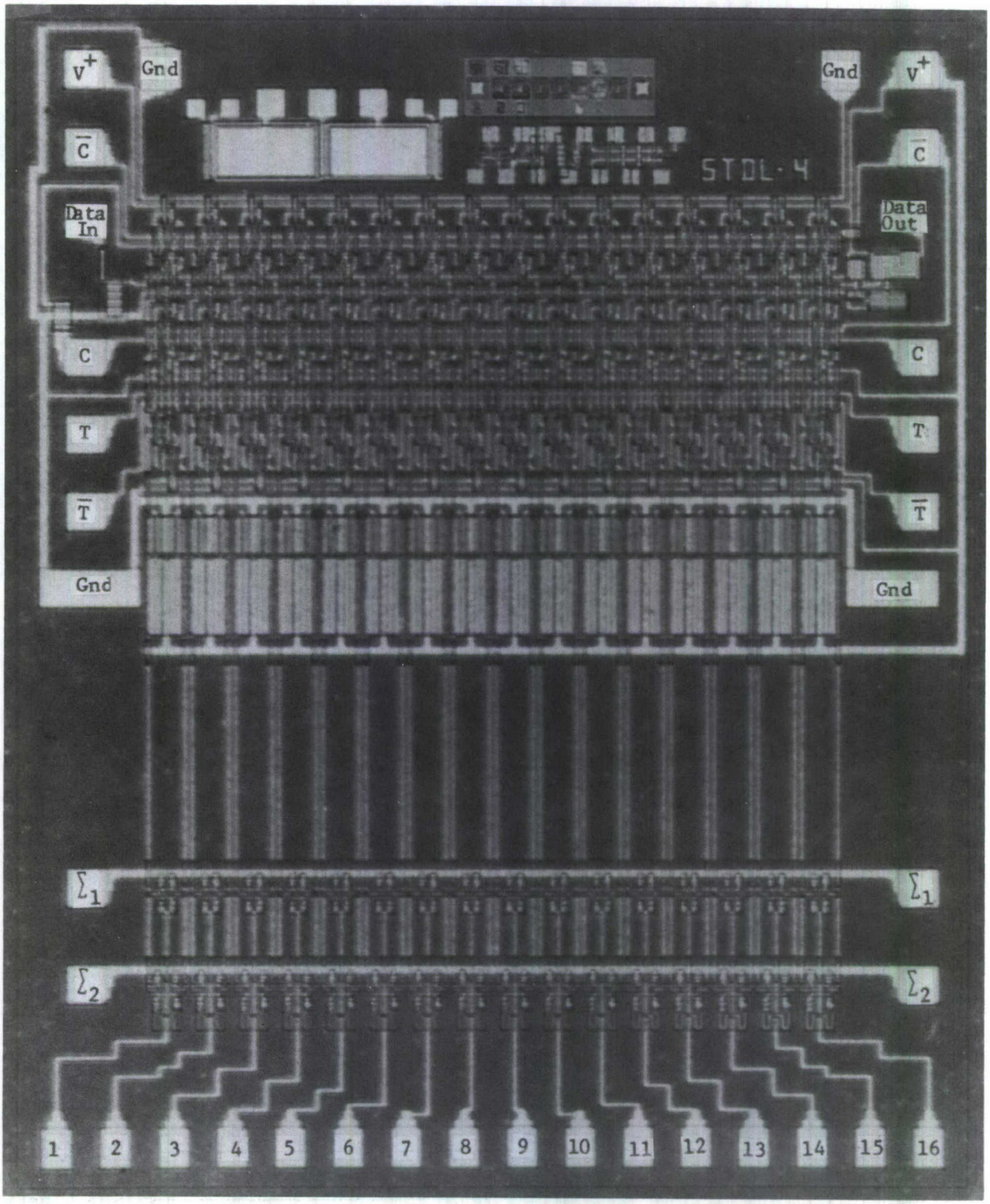


Figure 6. CMOS/SOS Integrated Circuit Die (Controls 16 Taps)

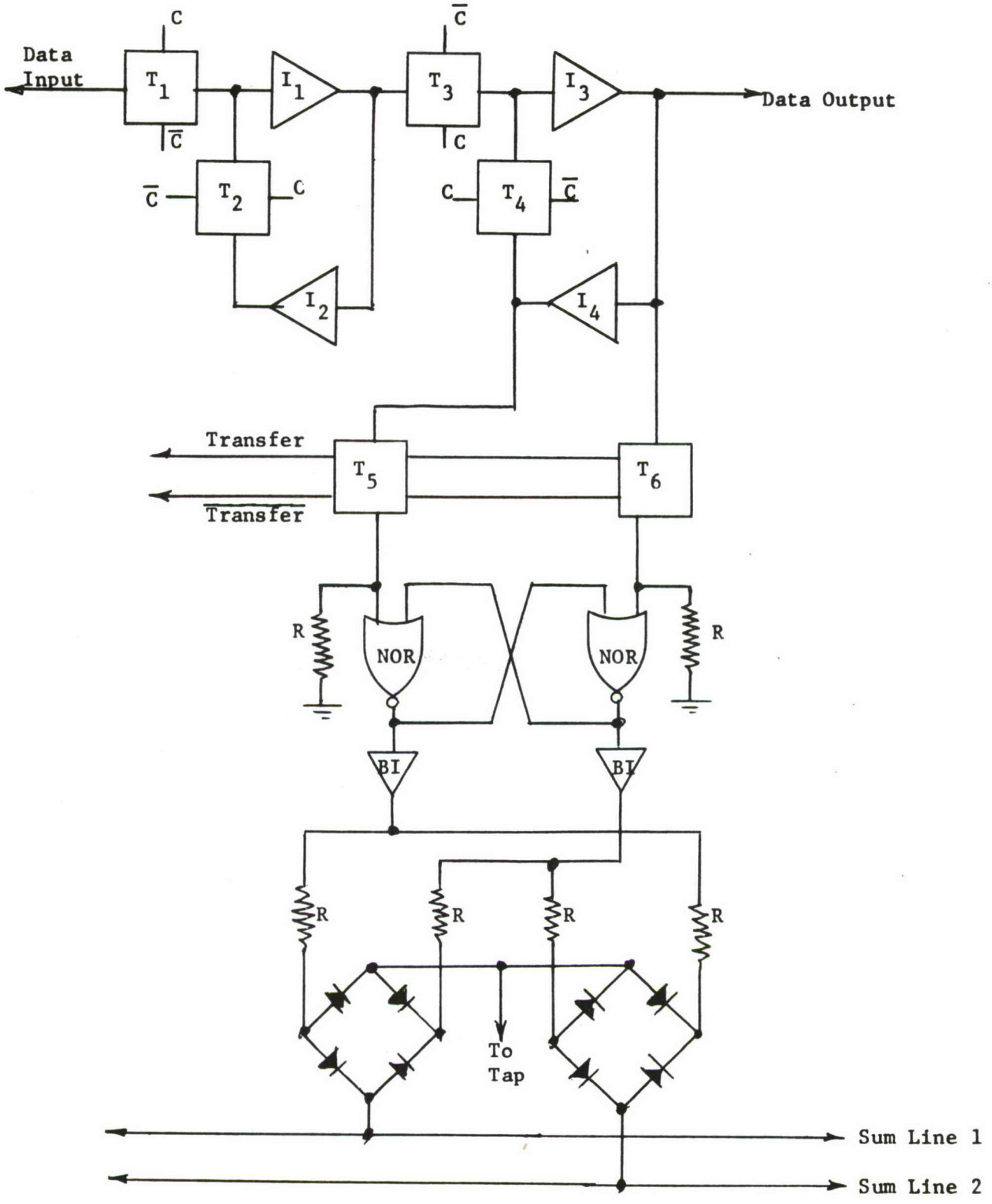


Figure 7. CMOS Tapped Delay Line Switch Cell

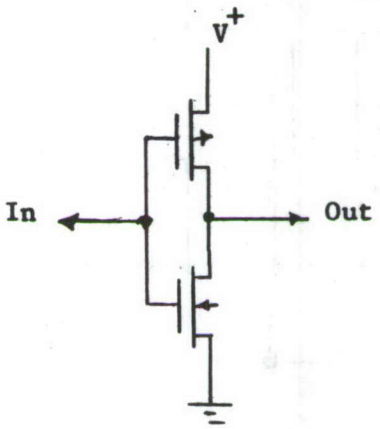


Figure 8. CMOS Inverter

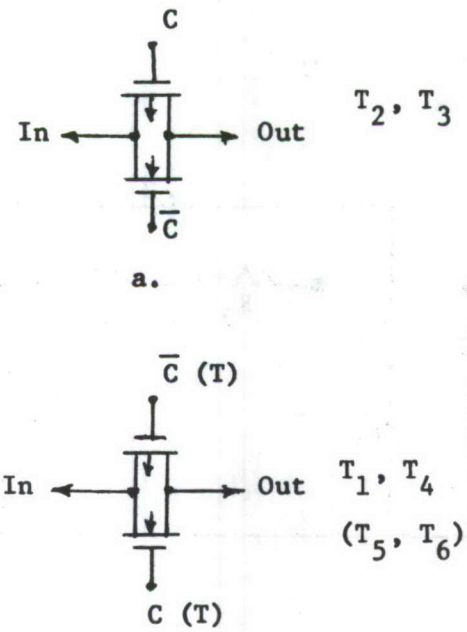


Figure 9. CMOS Transmission Gates

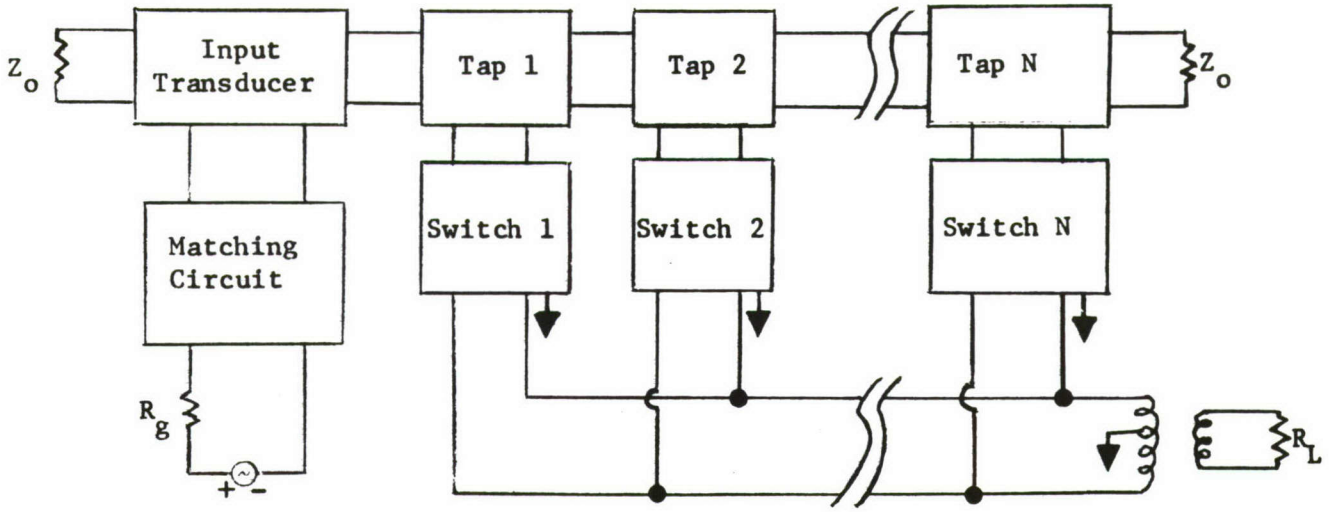


Figure 10. PTDL Model

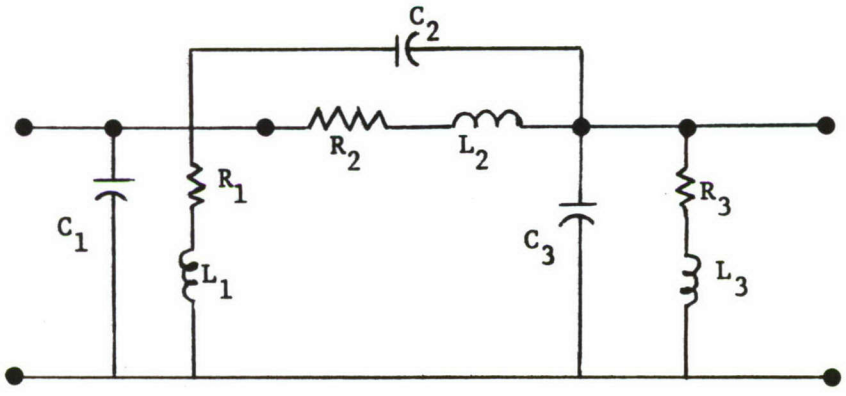


Figure 11. Input Circuit

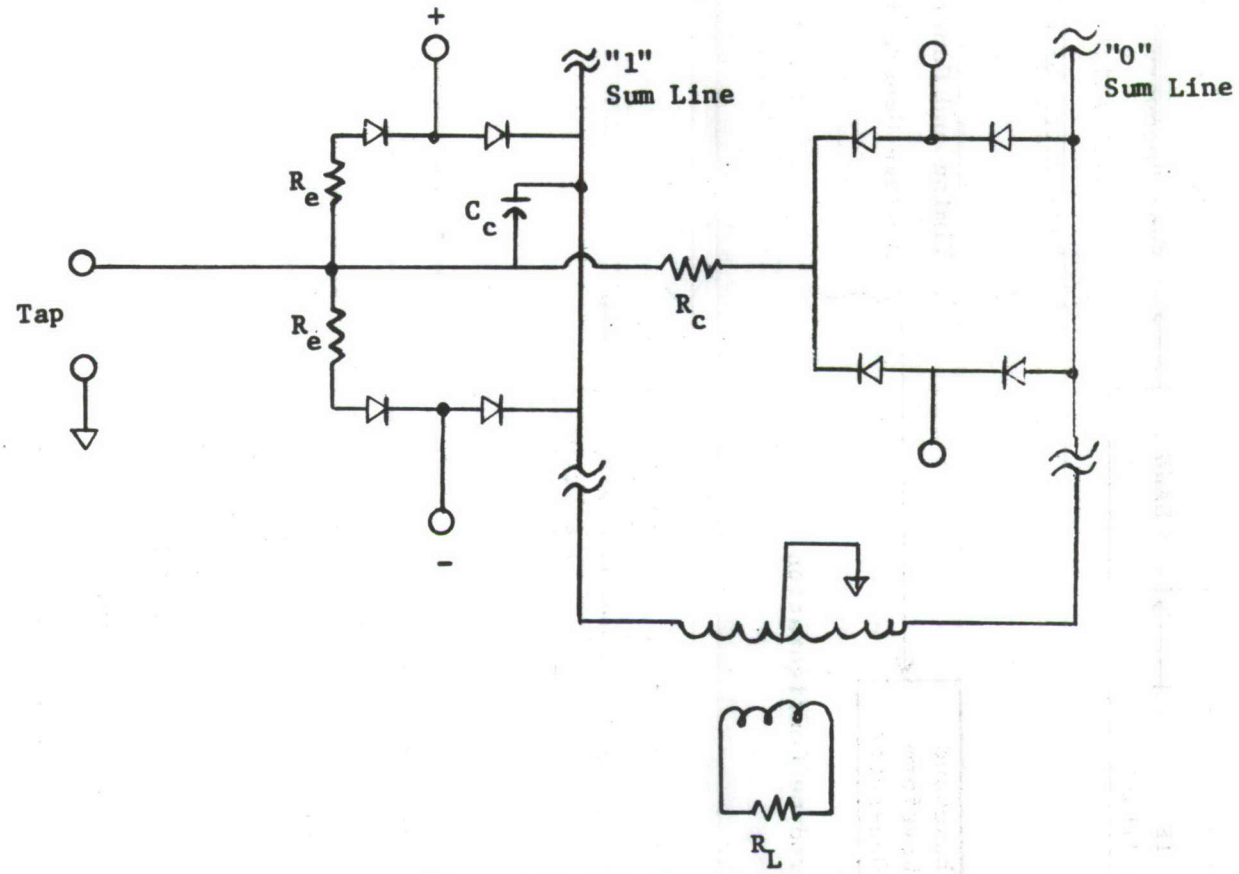


Figure 12. Tap Switch Model

The insertion loss from input transducer to the first tap for this case at 435 MHz was calculated to be 84 dB compared to the 72 dB predicted for the acoustic tapped delay line alone with no microelectronic circuit present.

Since the total signal delivered to the load is the sum of the individual current contributions from each acoustic tap then the insertion loss from a 127 chip spread waveform to the correlation peak (where the signals from all taps sum coherently) should be 84-20 $\log_{10}$ (127) = 41.9 dB. Assuming a +20 dBm input power limitation and a 20 MHz bandwidth (-101 dBm noise floor) the maximum dynamic range for this device should thus be ~ 70 dB when the necessary amplifier noise contributions are taken into account.

The sum line was not modeled as a transmission line in this case. The transmission line loading effects and their influence on device performance are discussed and analyzed in detail in Section 3.5 after the experimental results are presented in Section 3.4 and significant discrepancies between simple theory and experiment are noted.

2.5 CODED WAVEFORM GENERATION - ACTIVE VS PASSIVE

A task was included in this program with the objective of determining whether either active or passive coded waveform generation offered any overriding advantages in transceiver applications. Figure 13 shows two transceiver types which can be implemented using SAW devices.

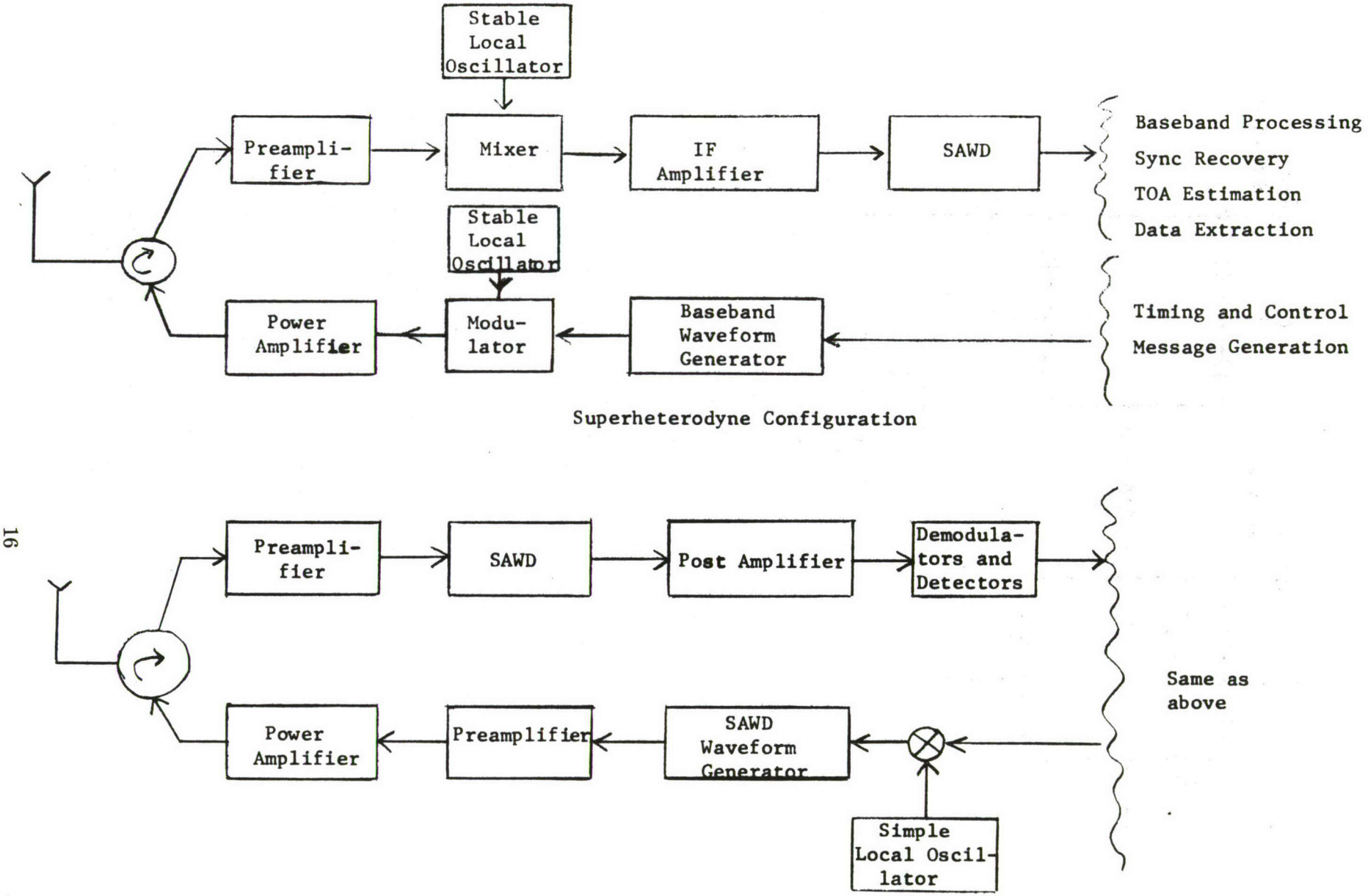


Figure 13. Transceiver Types Employing Surface Wave Processors

Initial inspection of these two possibilities indicates the direct technique appears to have fewer components and may have sensitivity or dynamic range advantages since mixer losses in the receiver are not experienced.

However, a complete analysis to determine which is the better technique would necessarily have to be narrowed down to a particular system operating with a specific waveform if it is to be meaningful. In addition the component count, cost, and reliability would have to be taken into account for the candidate system.

A task of this magnitude would obviously have been beyond the scope and intent of this program. The analysis on this task was therefore restricted to determining the limitations of the SAW tapped delay line when used to generate and correlate a phase coded spread spectrum waveform. Previous analysis determined that a major limiting factor for SAW devices was the orientation accuracy of the piezoelectric substrate, in this case ST quartz.

Since quartz is an anisotropic crystalline material, the acoustic surface wave velocity depends on the particular crystal plane and SAW propagation direction in that plane. Analytical programs used at Rockwell International and elsewhere (Ref 4) calculate, from the basic physical constants of the material, the surface wave velocity for any desired crystal plane and propagation direction. For satisfactory operation over a wide temperature range (-55 deg C to +80 deg C) ST cut quartz is used which has the orientation relations shown in Figure 14 with SAW propagation along the X axis in a plane at 42.75° to the Y axis. SAW phase and group velocities are collinear for this case, the first order temperature coefficient of delay is zero and the second order coefficient is small.

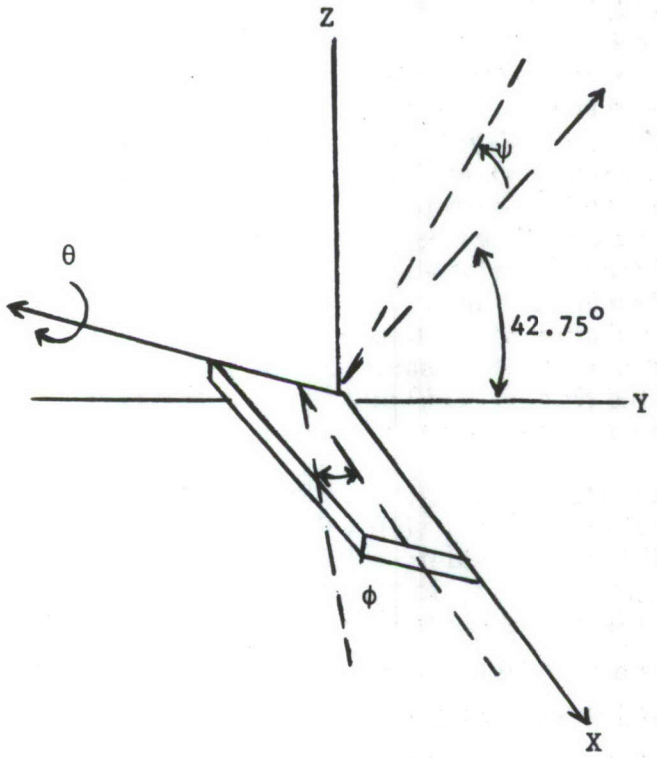


Figure 14. ST-Cut Quartz Orientation with Angles of Deviation θ, ϕ, ψ

In practice normal fabrication tolerances exist which cause small departures from the exact crystal plane and orientation when quartz bars are cut from large boules and one surface polished to an optical finish for interdigital transducer fabrication. Commercial suppliers of ST quartz bars normally only guarantee orientations of standard quartz bars within ±15 minutes of the required orientation although orientations can actually be measured to a maximum error of ±3 minutes. The consequences of this departure are shown in Figure 15. This figure shows the surface wave velocity deviation $\left(\frac{\Delta v}{v}\right)$ in parts/million (ppm) plotted as a function of crystal misorientation defined (see Figure 14) as small angular rotations about the surface normal (ψ), the direction of propagation (ϕ) and the axis perpendicular to the surface normal and the direction of propagation (θ). This will now be examined in detail in conjunction with Figure 16 which shows the loss in processing gain V_s velocity error for the tapped delay line of this program which has 2,667 acoustic wavelengths between the first and last taps (127 gaps x 21 wavelengths per gap). The total number of acoustic wavelengths in the tap array is a key factor in error analysis. This is illustrated by considering the fact that the phase difference between first and last taps (for a 2,667 wavelength path difference) caused by a 100 ppm velocity error is 2,667 x 100 x $360/10^6$ = 96 deg.

As will be seen from Figure 15 a maximum deviation from a true ST cut of ±15' implies a maximum velocity deviation of ±118 ppm (total). This figure is the maximum possible error in substrates within normal manufacturer's tolerances including a rotation of 15' about the z and y axes, in addition to the deviation from an ST-cut (rotation about the X axis of angle ψ in Figure 14). From the diagram it will be seen that deviation angles θ and ϕ have relatively small effect on the velocity compared to angle ψ. Further, this deviation from a true ST cut means that the first order temperature coefficient will no longer be zero. The variation of the first order temperature coefficient as a function of crystal orientation has been determined by Schulz, et al. (Ref 5). From these calculations it can be shown that a misorientation of ±15' will introduce a maximum error of approximately 40 ppm over a 145 deg C temperature range. Thus, the total maximum velocity or phase error introduced by a misorientation of the quartz substrate by ±15' over a temperature range of 145 deg C will be ±158 ppm. Consider the worst possible case of two quartz substrates with one bar misoriented +15' and the other misoriented -15'. If two delay lines are prepared by depositing identical transducer patterns on both substrates, the maximum possible deviation between the two devices over a temperature range of 145 deg will be 316 ppm. This much variation is not acceptable for most applications, as it implies a loss in processing gain of >10 dB as shown in Figure 16. It is usually desired that the loss of the processing gain be kept below 1 dB, and from Figure 16 this implies that the error can be no greater than 120 ppm.

The maximum error can be reduced to an acceptable level by careful transducer design. First, note that any velocity shift will produce a corresponding frequency shift for a given transducer. Consider, for example, a transducer designed to have a center frequency $f_o = v_o/\lambda$ where v_o is the SAW velocity for a perfectly oriented ST cut bar. If the bar is misoriented in the positive direction the surface acoustic wave velocity is increased to a new value $v = v_o + \left(\frac{\Delta v}{v_o}\right) v_o$, where $\frac{\Delta v}{v_o}$ is the error in ppm determined from Figure 16. For this orientation the center frequency of the transducer will no longer be f_o but have the value $f_2 = \left[v_o + \left(\frac{\Delta v}{v}\right) v_o \right] /\lambda = f_o + \Delta f$. If, however, it is desired that the transducer deposited on the new crystal

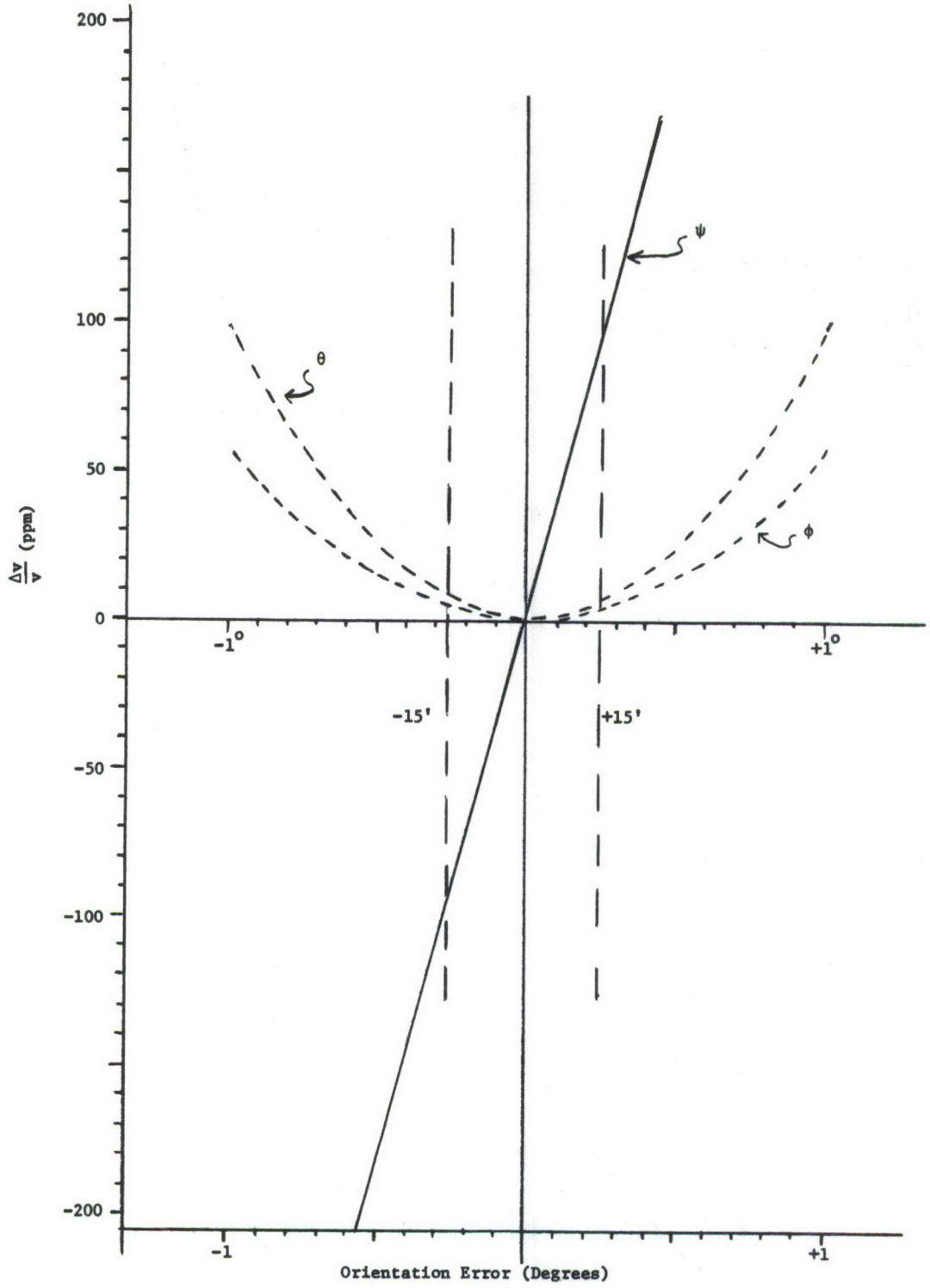


Figure 15. SAW Velocity Deviations in Parts Per Million (ppm) for Small Deviations from ST Quartz Orientations

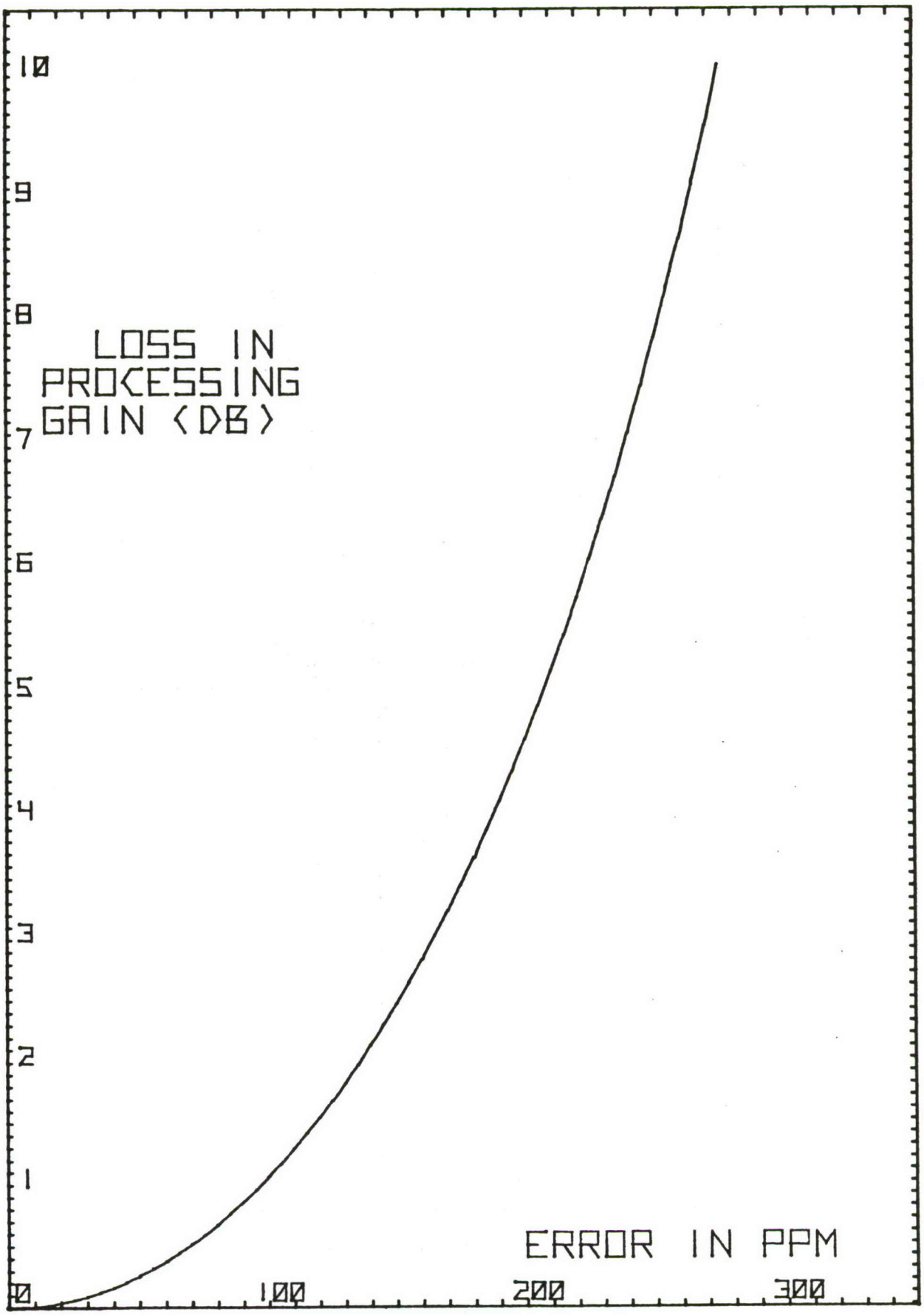


Figure 16. Loss in Processing Gain vs Error in ppm for a TDL with 2667 Wavelengths Between First and Last Tap

orientation have the same center frequency as the transducer on the original orientation, a new transducer mask will be required. A new transducer can be readily designed by using a new value for the wavelength. In other words the relation

$$f_2 = \frac{\left[v_o + \left(\frac{\Delta v}{v}\right) v_o\right]}{\left[\lambda + \left(\frac{\Delta\lambda}{\lambda}\right)\lambda\right]} = f_o$$

must be satisfied. If the transducer designed to have center frequency f_o on the rotated substrate were deposited on the unrotated crystal the center frequency would be less than f_o since for this case

$$f = \frac{v_o}{\left[\lambda + \left(\frac{\Delta\lambda}{\lambda}\right)\lambda\right]} < \frac{v_o}{\lambda} = f_o.$$

In short in order to compensate for the upward frequency shift due to a positive misorientation of the crystal, a new photomask must be designed with a center frequency less than f_o on the original orientation. Similarly, for negative misorientations the center frequency must be slightly increased.

Thus, in principle, errors due to misorientation can always be compensated for by designing another photomask for each crystal orientation. If a large number of groups of substrates are involved, however, it is not economically feasible to fabricate a separate photomask for every orientation group. It is more convenient to divide the total number of substrates into a small number of groups with each group covering a range of crystal orientations. Then a photomask can be designed for each group which will hold the error of the individual members to a specified tolerance. Of course, the smaller the tolerance, the greater the number of individual transducer photomasks required. For example, it has been determined at Rockwell that for a moderate number (~20) of wavelengths tap spacing, an acceptable tolerance of ±47 ppm can be achieved for all substrates with random orientation errors of ±15' from ST orientation by the use of four masks.

By utilizing the technique described above, errors arising from substrate misorientation can be held within tolerable limits. Errors arising from temperature variation (Ref's 4 and 6) must now be considered. As discussed previously, the first order temperature coefficient should introduce no more than 40 ppm error over a temperature range of 145 deg C on a crystal misoriented by ±15'. Thus, a given substrate with a maximum deviation of ±47 ppm from f_o, due to misorientation, will have a total maximum deviation of ±87 ppm from f_o when the first order temperature coefficient over a temperature range of 145 deg C is included.

The final major source of error arises from the second order temperature coefficient. The second order temperature coefficient for ST quartz over a large temperature span is not zero, and the deviation from center frequency due to second order effects, although small, must be included in the overall device performance specifications. Experimental evaluations of temperature effects on ST quartz TDL's at Rockwell International yielded the data on which the following results were based. This data agrees with similar data from other sources (Ref's 4 and 6). The combined

effect of both first and second order temperature coefficients on a 128 tap TDL with 21 wavelengths spacing between taps, was used to prepare Figure 17 which shows the worst case or maximum loss in processing gain vs temperature for several device design approaches. Curve A illustrates the maximum loss in processing gain which could arise if the design considerations discussed in this section were ignored and one SAW TDL was used to generate a coded waveform with another SAW TDL used as the matched filter. This curve assumes one substrate is misoriented +15', the other misoriented -15' and transducers designed for a true ST-cut (no misorientation) substrate employed on both lines. In this case the full range limits of +158 to -158 are operable and an error of 316 ppm has to be taken into account. As will be seen from the figure, the loss in processing gain for such a device is completely unacceptable. Curve B assumes the misorientation is again ignored, but here digital/LO code generation is assumed with frequency and chip rate accuracies of < 2 ppm. Only one SAW TDL is used as a matched filter for this waveform. For this case the combined maximum misorientation and first order temperature coefficient is only 158 ppm. The loss in processing gain is consequently reduced considerably from the previous case but is still above acceptable limits over most of the temperature span. Curve C shows the maximum loss in processing gain vs temperature (assuming digital code generation) for devices designed as discussed above; i.e., the velocity shift due to misorientation has been reduced to no more than ±47 ppm by dividing the substrates into orientation groups and designing a different transducer for each group. The maximum possible deviation from f_0 MHz due to both velocity errors and first order temperature coefficient is therefore ≤ 87 ppm. As will be seen from the curve, the maximum loss of processing gain due to orientation errors and both first and second order temperature effects is <1 dB over the temperature range from -25 deg C to +85 deg C. The loss in processing gain vs frequency is also strongly dependent on the tap spacing and the number of taps, or in other words, on the length of the tap structure in wavelengths. This is illustrated in Figure 18 where loss in processing gain is plotted as a function of temperature for a number of tap spacings, assuming a 128 tap line on a substrate with minimum orientation deviation.

Obviously reducing orientation tolerances on ST cut quartz bars would allow longer TDL's to be fabricated with acceptable processing gain over a wider temperature range. Figure 19 shows the worst case loss in processing gain predicted for the PTDL's developed on this program as a function of crystallographic misorientation tolerances (from 0' to 7.3').

The worst case design curves presented in this section define some practical limits for SAW device performance which can be related to actual systems waveforms when operating temperature environments are specified. As such they help in defining what phase coded waveforms can be expeditiously generated by impulsing SAW TDL's without accepting undesirable loss in processing gain on correlation. In addition the tolerances required on crystallographic orientation and temperature versus processing gain for specific waveforms can be defined to allow realistic cost/performance tradeoff studies to be made.

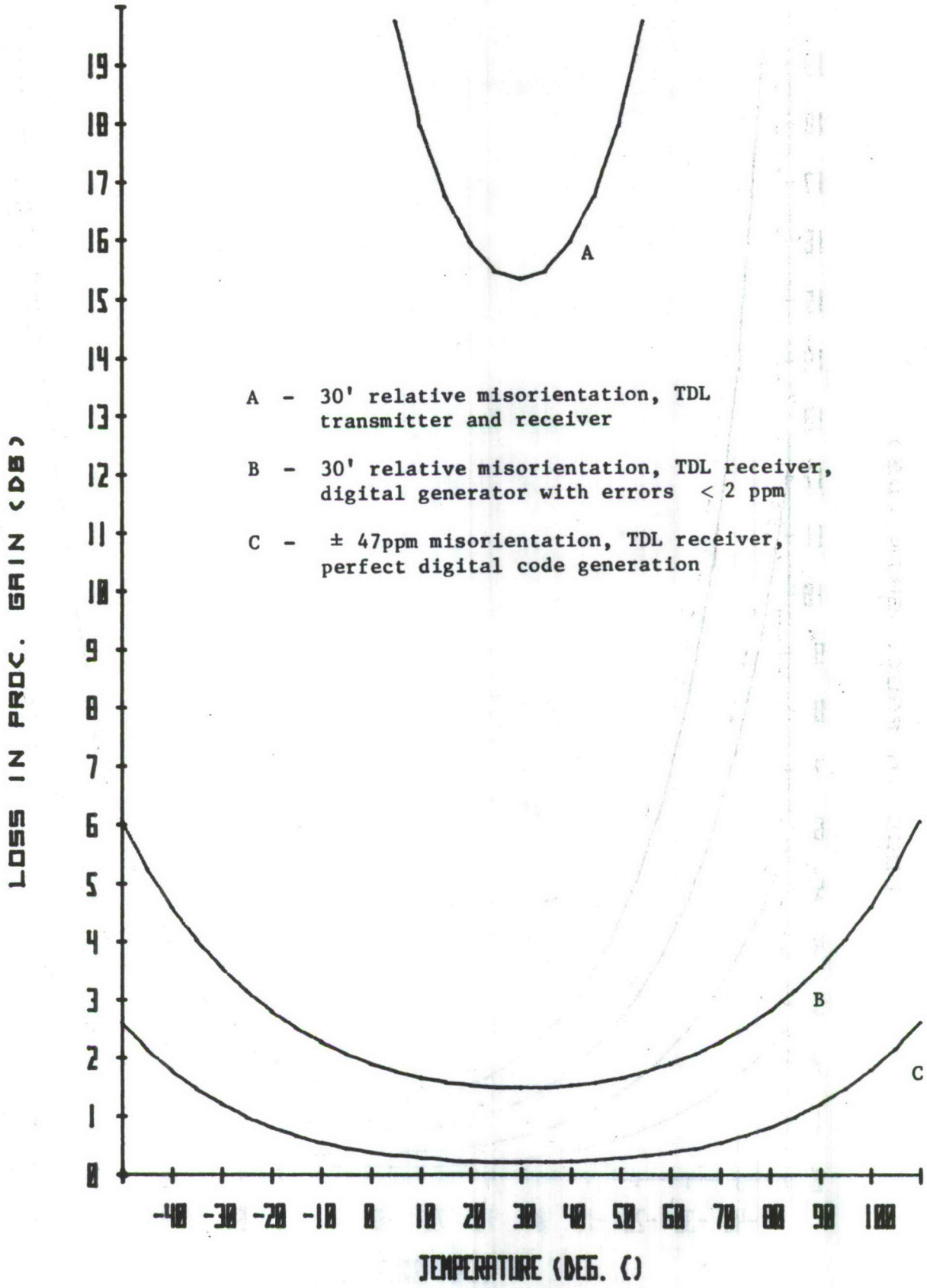


Figure 17. Loss in Processing Gain vs Temperature for a SAW TDL with 2667 Wavelengths Between First and Last Taps

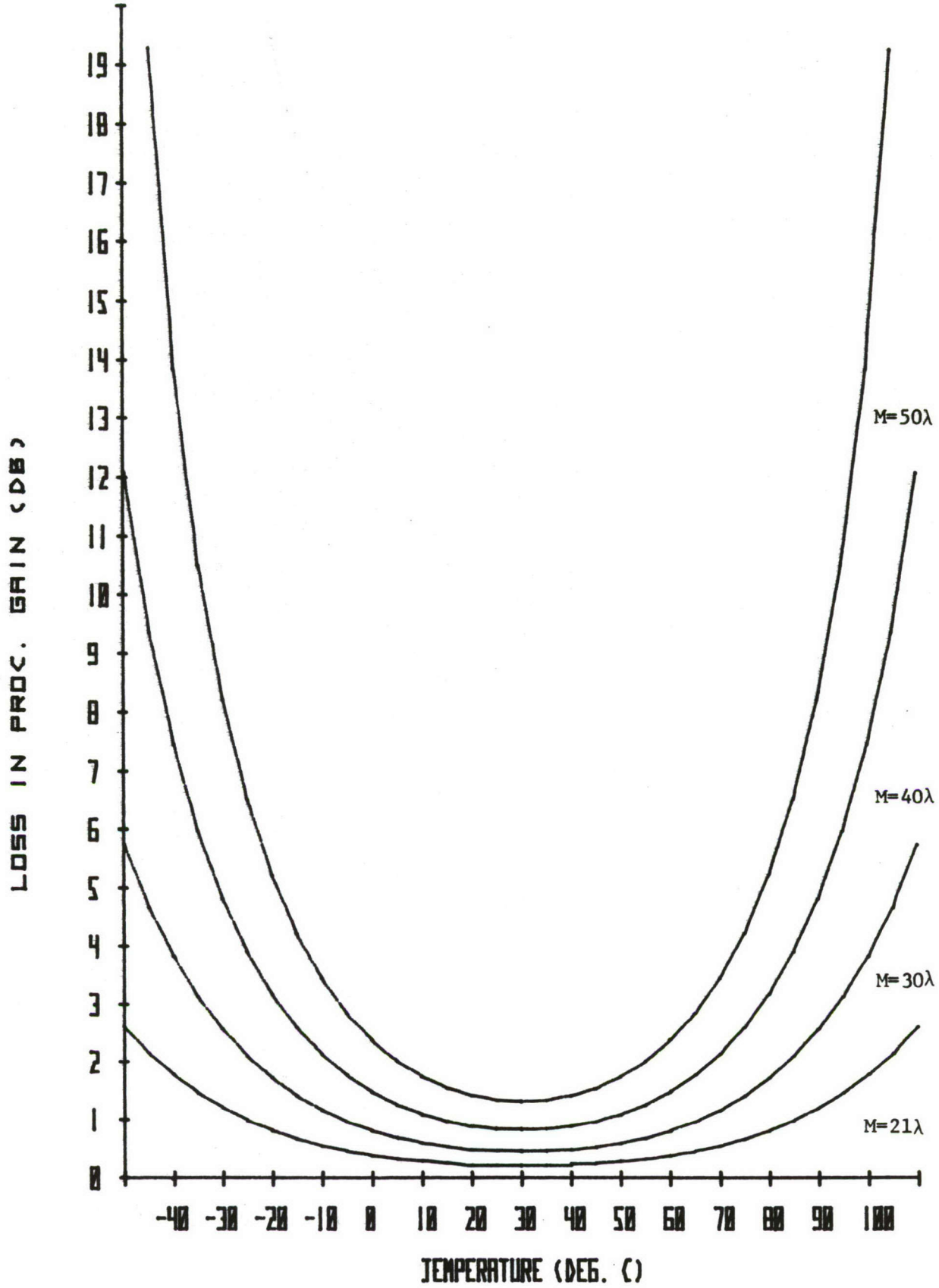


Figure 18. Loss in Processing Gain vs Temperature for a SAW TDL with 128 Taps as a Function of Tap Spacing M (in wavelengths)

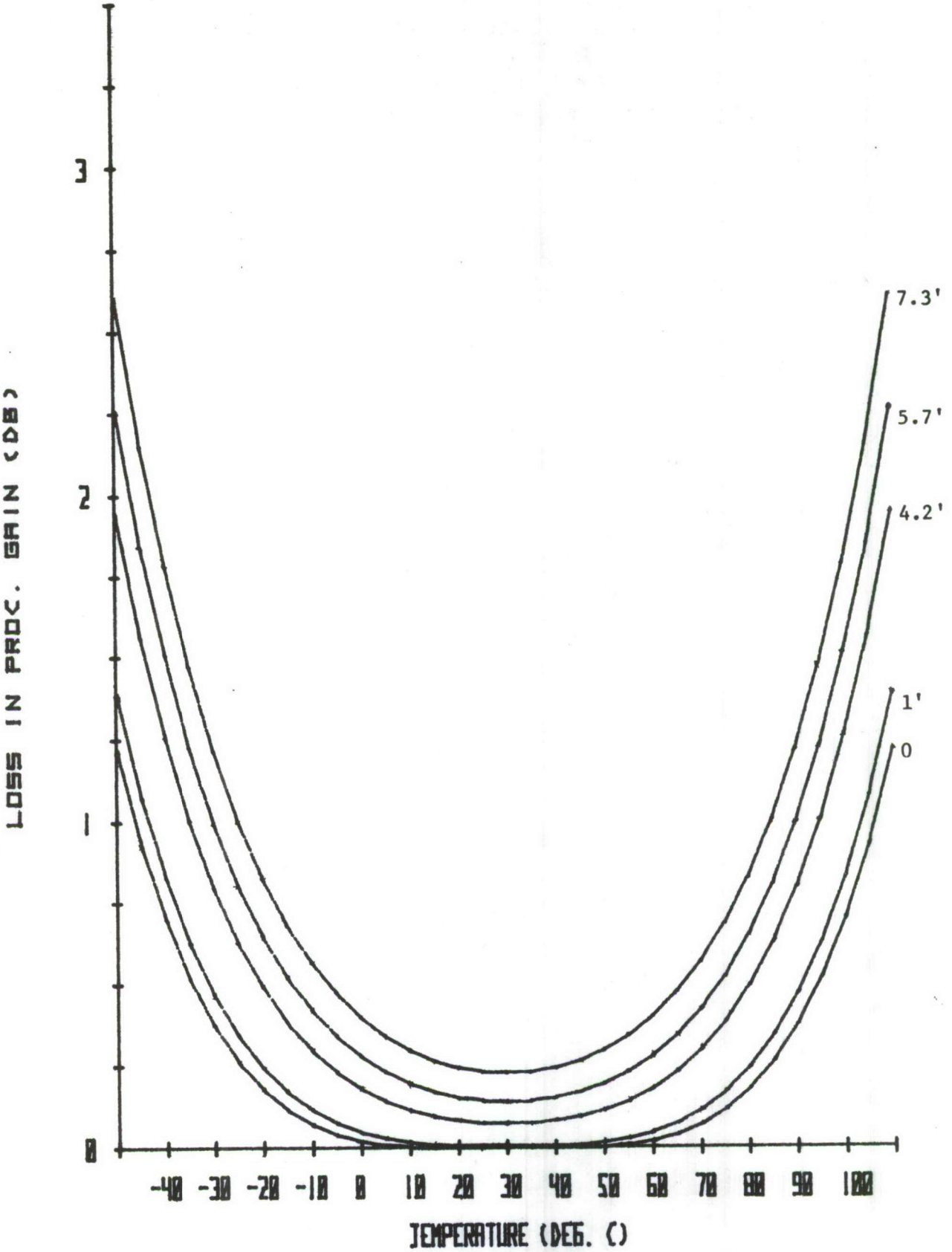


Figure 19. Loss in Processing Gain vs Temperature for Small Deviations from ST Quartz Orientation. The curve 0^{o} deviation represents the effect of the second order temperature coefficient alone.

3. FABRICATION AND EVALUATION OF 435 MHz PTDL'S

3.1 INTRODUCTION

The following Sections 3.2 and 3.3 describe the fabrication techniques used and problems encountered on the acoustic and microelectronic IC portions of this program respectively.

Section 3.2 contains experimental results on the acoustic tapped delay line without the integrated electronic switching circuits to allow comparison with the theoretical predictions of Section 2.2. All 128 taps on this device were connected to bonding pads on both sides of the tap array.

Sections 3.4 contains details on the performance of the complete PTDL assembly and a comparison of theory and experiment. Section 3.5 analyzes lossy transmission line effects in the microelectronic integrated circuits.

3.2 ACOUSTIC TAPPED DELAY LINE

Fabrication techniques for the acoustic tapped delay lines on this program were conventional SAW device fabrication procedures with some minor changes. Figure 20 shows the acoustic tap array (128 taps) on an ST quartz bar with wire connections to the eight CMOS/SOS integrated circuits. The angled fan-out pattern on the tap array is obviously needed to line up the taps with the bonding pads on the CMOS/SOS integrated circuits.

A two step fabrication procedure was used to obtain the TDL. First a thin (800Å) aluminum film was evaporated on the quartz bar and the transducer finger structure defined in this film with conventional positive resist (Shipley 1350) and chemical etching techniques. The fan-out pattern and bonding pads were then applied by a lift-off process using positive resist and a 5,000Å thick aluminum film. This particular processing sequence was necessary to ensure that only thin aluminum was used in the acoustic path to reduce dispersion and mechanical reflection effects while a sufficiently thick aluminum was available at the bonding pads to ensure that ultrasonic aluminum wire bonding could be used to connect IC chips and delay line transducers.

Several other procedures were investigated such as applying the pads first and then obtaining the fingers by a lift-off procedure. Lack of metal continuity at the edge between the thin finger and the thick bonding pad proved to be a severe problem with that approach.

To compare the actual SAW tapped delay line performance with theoretical predictions without the complicating presence of the microelectronic IC several TDL's were fabricated with all the tap bonding pads connected together. Figure 21(a) shows the TDL output with a gated 435 MHz input signal. Four open taps caused by breaks in the tap fingers are apparent in this waveform. An insertion loss measurement was obtained by using a 75 nsec RF pulse and measuring the insertion loss (L) to a 50 ohm load by attenuator substitution. The insertion loss to a single tap is then (L+6) dB since a 75 nsec pulse results in the coherent addition of the output currents from two adjacent taps 50 nsec apart and hence a single tap response would be 6 dB lower. The insertion loss determined in this way was 72 dB to a single tap - in good agreement

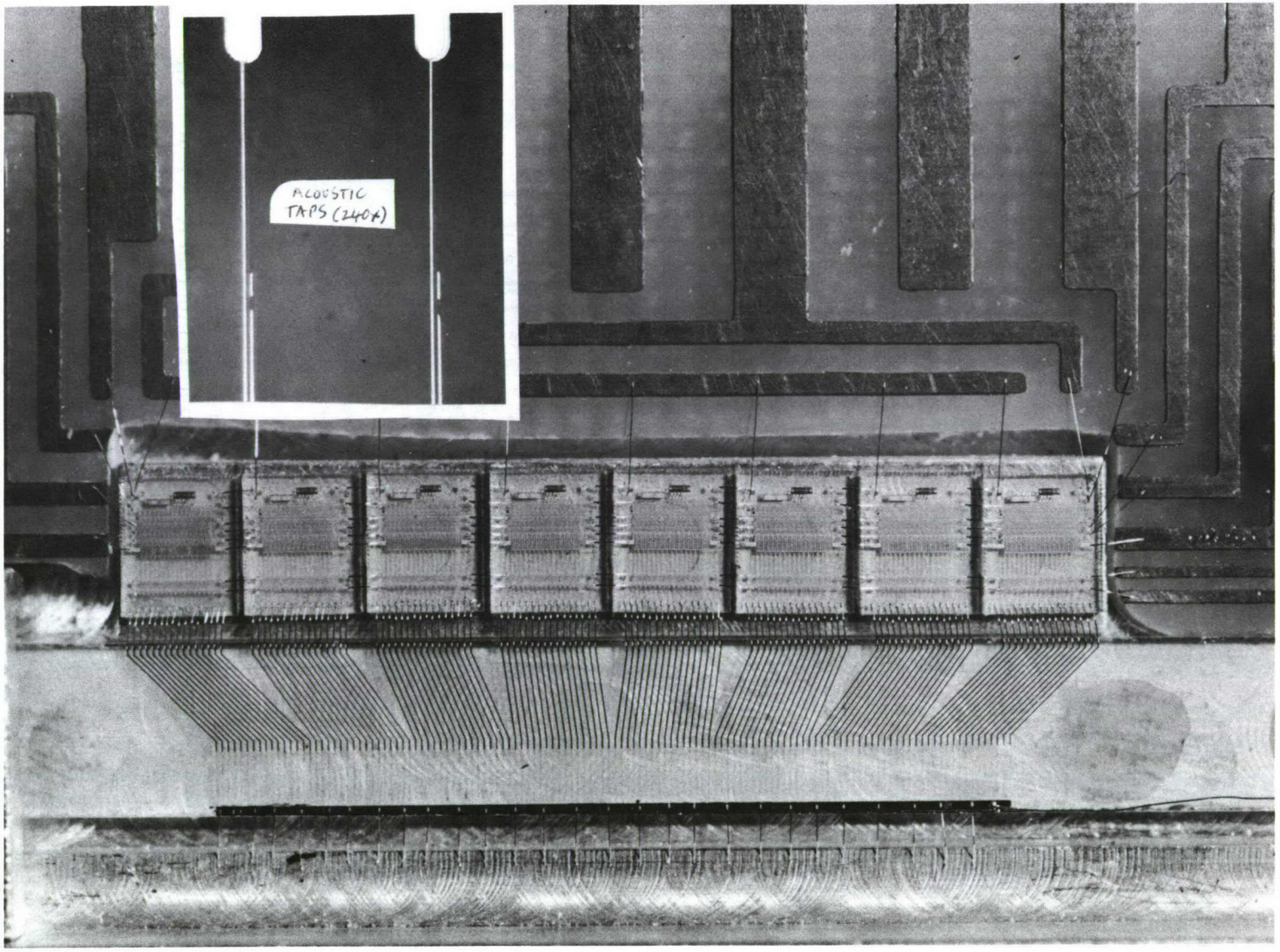
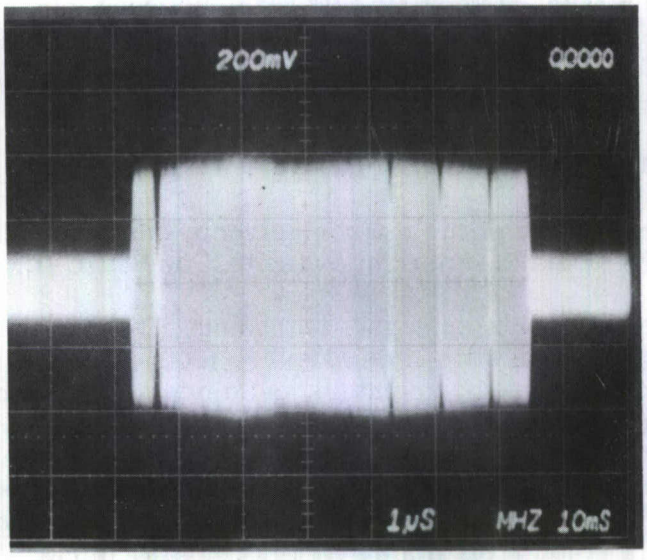
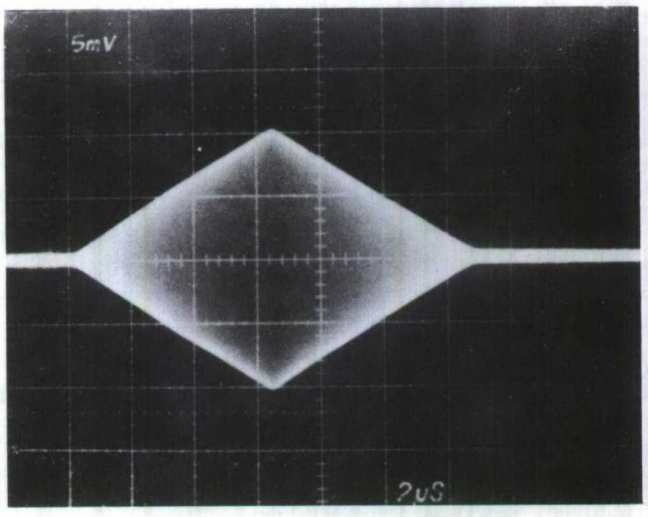


Figure 20. 435 MHz Programmable Tapped Delay Line (128 Taps, 20.7 MHz BW)



(a)



(b)

Figure 21. Impulse Response of 128 Taps Linearly Apodized 435 MHz Tapped Delay Line (4 taps missing)

with theoretical prediction of Section 2.2. The 2:1 linear finger overlap apodization is also seen to compensate reasonably accurately for the losses at 435 MHz and give a uniform tap output. Figure 21(b) shows the response to an RF pulse equal to the delay between first and last taps. Excellent coherence between tap outputs results in an almost perfect triangular envelope. The input transducer is tuned by a single toroidal inductor. Figure 22 shows the input impedance as a function of frequency over the 415 to 455 MHz range.

3.3 SEMICONDUCTOR INTEGRATED CIRCUIT FABRICATION

The particular version of the microelectronic integrated circuit developed for use on this contract is referred to in the following text as STDL-4.

Silicon nitride self-registered gate technology (Ref 1, 2) has been utilized for processing STDL-4 CMOS on silicon on sapphire (SOS) circuits. The STDL-4 circuit consists primarily of CMOS shift registers and diode switching circuits having a chip size 0.115 x 0.134 in.

The final processing sequence used is shown in brief form in Figure 23. The starting SOS material throughout the program has been 1μm silicon films (±10 percent) of 10Ω-cm (±25 percent) on 2 in. diameter by 0.014 in. thick ($1\bar{1}02$) sapphire substrates obtained from Union Carbide or Inselek. The as-received SOS wafers are given an appropriate cleaning* then approximately 3000Å of thermal oxide is grown in steam at 1000 deg C. Negative photoresist is spun on the wafers and the P-wells are defined. The oxide in the P-wells is etched and the resist stripped. The wafers are given an additional steam oxidation at 1000 deg C to grow about 1000Å of oxide in the P-wells. This is to prevent surface contamination and channeling at normal incidence during boron implantation. Thick negative photoresist is applied and the P-wells are redefined. The photoresist (~1.5μm) plus the 3000Å oxide in the field act as an implant mask. Boron ions are next implanted into the P-wells through the 1000Å oxide layer at normal incidence. Implanting the P-wells before the islands are defined usually results in more uniformly doped wells and eliminates any possible edge effects which may arise. The dose and energy normally used have been 8×10^{-12} cm^{-2} at 200KEV. After implantation the photoresist is stripped and the wafers are given a diffusion drive at 1000 deg C for 3 hours in nitrogen. Positive photoresist is applied and the islands are defined. The oxide in the field is etched, then the resist is removed. The thermal oxide remaining over the islands acts as a mask against the KOH silicon etch. The islands are etched in a solution of 6N KOH and isopropyl alcohol at 60 deg C. Once the islands are defined, the oxide over the islands is etched. 500Å of thermal oxide is next regrown in steam at 875 deg C and then 500-600Å of silicon nitride is deposited on the wafers.

*The wafers were cleaned as follows:

1. Wafers spin swabbed with DI water.
2. 10% HF dip and DI H_2O rinse.
3. Cleaned in a solution of $H_2SO:H_2O_2$(1:1) at ~100 deg C for 5 minutes and rinsed in DI H_2O.
4. Cleaned in a solution of $H_2O:HC1:H_2O_2$(6:1:1) at ~85 deg C for 5 minutes and rinsed in DI H_2O.

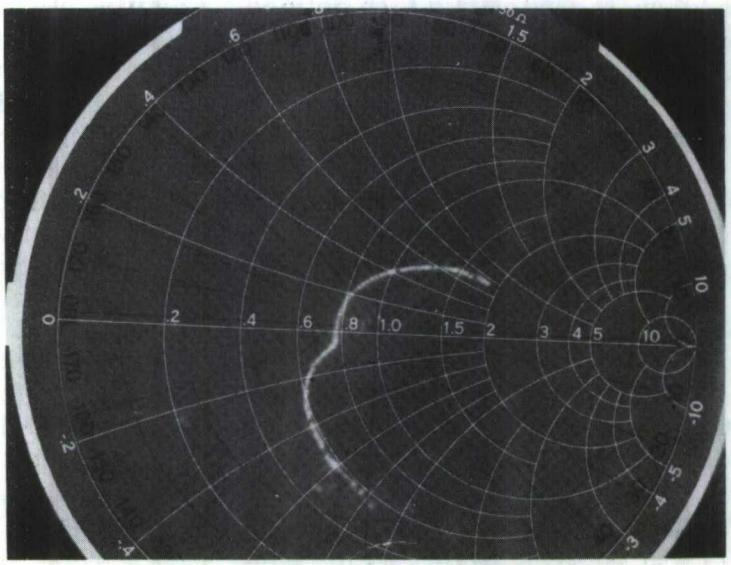


Figure 22. Input Impedance of 435 MHz TDL (415 MHz - 455 MHz Sweep)

1. P-well definition, boron implant and drive
2. Island definition
3. Oxide growth and silicon nitride deposition
4. Gate definition
5. Boron diffusion
6. Phosphorus diffusion
7. Open contacts
8. Metalization
9. Metal Protection and sinter

Figure 23. Processing Sequence for STDL-4 Circuits

Since photoresist does not adhere well to silicon nitride surfaces a thin oxide layer is grown in steam for 10-20 minutes at 1000 deg C. Shipley 1350J photoresist is spun on the wafers and the gates are then defined. The unwanted nitride/oxide is etched in a solution of stabilized fluoboric acid mix and phosphoric acid** at 105-110 deg C. The resist is stripped and thermal oxide in steam at 1000 deg C is again grown in those regions not protected by nitride/oxide layers. Negative photoresist is applied, the P^+ regions defined, and the oxide is etched from these regions. The resist is stripped and boron predeposition is carried out at 1000 deg C. Oxidized boron nitride wafers (Ref 3) have been used as the source for boron. After deglazing the wafers, boron is diffused in a steam ambient at 1000 deg C. Negative photoresist is used, the N^+ regions defined and the oxide is etched from these regions. The resist is stripped and phosphorus predeposition is carried out at 950 deg C with $POC1_3$ as the source. The wafers are deglazed and subsequently diffused in steam at 1000 deg C. Again negative photoresist is applied, the contact areas defined, and the oxide etched from these regions. 1.2μm of aluminum is evaporated onto the wafers which are mounted on a rotating planetary holder and maintained at about 270 deg C in order to obtain adequate step or island edge coverage. Shipley 1350J photoresist is spun on the wafers and the metal defined. The unwanted aluminum is etched off and the resist stripped. For metal protection 4000-5000Å of silox (low temperature SiO_2) is deposited on the wafers, positive resist applied and the metal contact pad areas defined. The silox in the pad areas is etched and the resist stripped. The wafers are finally sintered in nitrogen or forming gas at 465 deg C.

The following main problems were encountered before the process sequence and photomask set were finalized.

- Variability in silicon nitride etching
- Poor photoresist adhesion to silicon nitride
- Irregular silicon island edge profile
- Insufficient deglazing after predeposition
- nonoptimum ion implant doping
- Photomask errors

The nature of these problems and the solutions developed on this program are as follows. The gate channels in the early runs were defined by depositing a silox layer over the nitride and densifying it in O_2 at 1000 deg C. After masking the unwanted silox was etched and the underlying nitride etched in an ammonium dihydrogen phosphate ($NH_4H_2PO_4$) melt[4] at 210-220 deg C. However, this etch was not consistent resulting in the loss of silox masked nitride in the gate channels or unwanted nitride remaining. Therefore, this silicon nitride etch was rejected and the stabilized fluoboric acid mix

**The nitride etch is prepared in the following way: To each 100cc of phosphoric acid is added 1.5cc of stabilized fluoboric acid mix. The fluoboric acid is stabilized by adding 2 grams of boric acid crystals to each 25cc of fluoboric acid.

and phosphoric acid was used in its place. The advantages of this latter nitride etch were the lower etching temperature, the elimination of the silox layer and the use of positive photoresist as a mask for the etchant. Also, as discussed previously, photoresist adhesion to a bare or as-deposited silicon nitride surface was found to be poor. By oxidizing the surface, a thin layer of SiO_2 is formed which improved resist adhesion considerably. The oxide film thickness formed over the nitride was determined on control bulk silicon wafers on which silicon nitride films were deposited. The nitride thicknesses were measured with an ellipsometer and then the wafers were oxidized in steam at 1000 deg C for various times. The oxide formed was stripped and the nitride thicknesses remeasured. The difference between the initial and final thicknesses was assumed to be the SiO_2 thickness and this dependence as a function of time is shown in Figure 24. It is seen that the SiO_2 formed over the nitride is quite thin but is essential for photoresist adhesion.

Early in the program the silicon islands on sapphire were etched in a solution of 6N KOH in methyl alcohol. Usually the islands etched with this solution resulted in tapered edges; however, in some runs the island edges were notched as shown in Figure 25. This notch in the islands makes metal step coverage impossible. Figure 26 shows an example of open aluminum metal over an island edge due to either notching or a gap between the N^+ oxide and the sapphire interface. (See subsequent discussion and Figure 29.) The islands in subsequent runs were etched in a solution of 6N KOH with isopropyl alcohol which consistently gave nice tapered island edges as shown in Figure 27. Figure 28 is a SEM showing excellent metal step coverage over a tapered island edge. Figure 29 is a SEM showing the N^+ Region after drive in an oxidizing atmosphere.

The first wafer lot that gave operational circuits was lot 105. In this and preceding runs the gates were regrown after the N^+ diffusion drive. That is, the nitride/oxide layers over the gate regions were etched and a new channel oxide was regrown. However, for the boron P-well implants used it was found that the leakage currents of the N channel MOS devices were higher than desired (~2-10μamp at V_D = 10v). (The leakage current of P channel devices was usually low, $\leq$0.01μamp at V_D = 10v. However, the lowest leakage (~0.01μamp) has been obtained by leaving the original nitride/oxide gate intact. Several processing steps and time can be saved by not having to regrow the gate oxide. Therefore, in subsequent runs the circuits were processed leaving the original nitride/oxide gate dielectric.

Another problem contributing to low circuit yield was traced to the diode switches and the gate protection diodes. The diode switches, the P^+N^+ test diodes and the gate protection diodes on a number of wafers were conducting excessively under bias. Originally, the diodes were formed by diffusing boron through the entire island and then masking stripes (for the protection devices) and half of the P^+N^+ diode islands, etching the oxide and diffusing phosphorus through the P^+ regions. The causes for the diodes shorting are believed to be: (1) insufficient deglazing after the phosphorus predeposition step and (2) insufficient diffusion time during phosphorus drive. If the wafers are not deglazed enough it is possible for phosphorus to remain between the P^+ oxide and sapphire interface and short out the P^+ regions after the drive in step. Assuming that deglazing is complete, then if phosphorus does not reach the sapphire interface, the junction area becomes much larger than intended and would cause excess leakage current. Since the P^+ region through which the phosphorus diffuses is doped to about 10^{19} cm^{-3} or greater diffusion to the sapphire interface takes considerably longer than when the base concentration is less. By increasing the phosphorus drive time it has

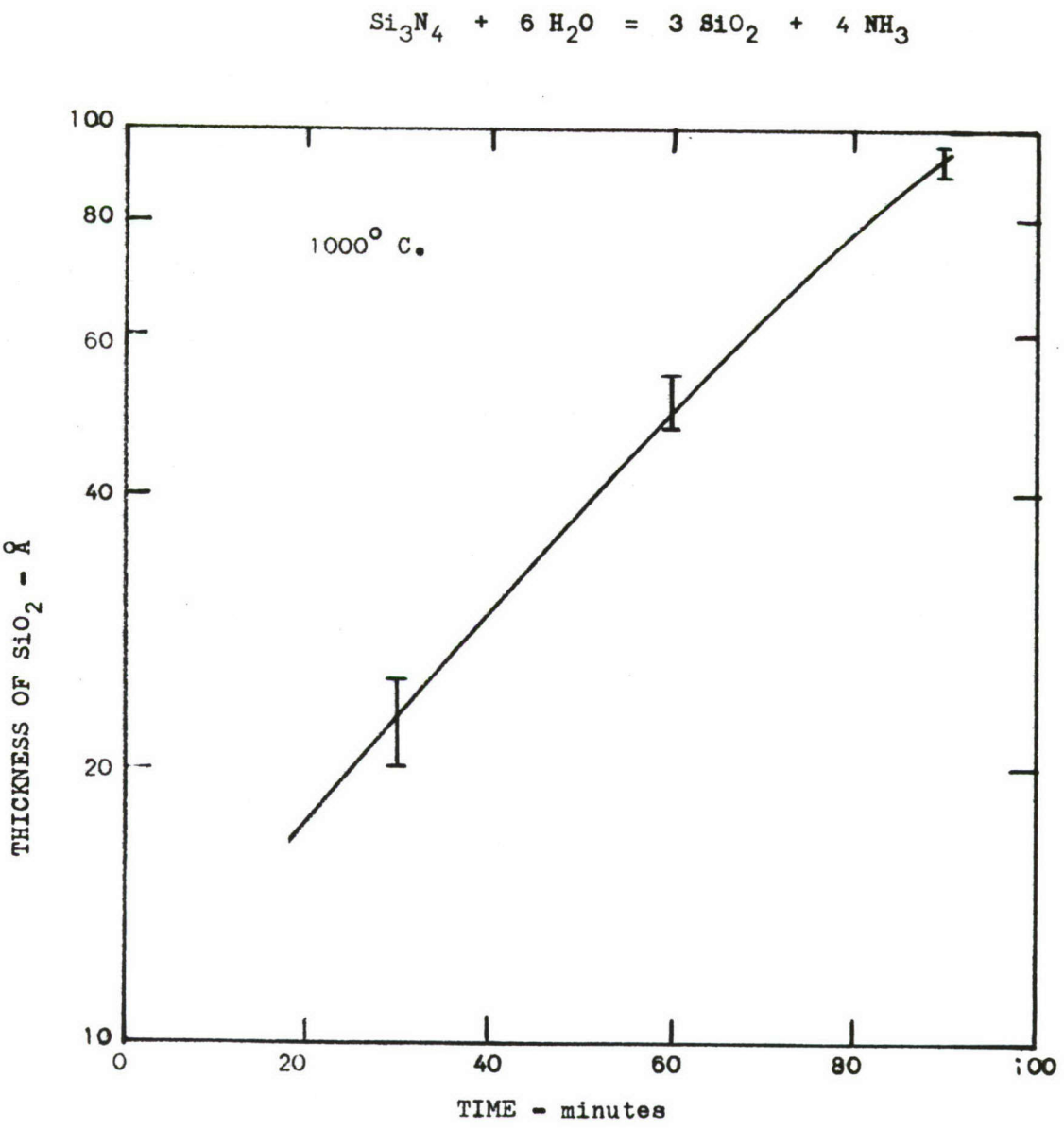


Figure 24. Steam Oxidation of Silicon Nitride

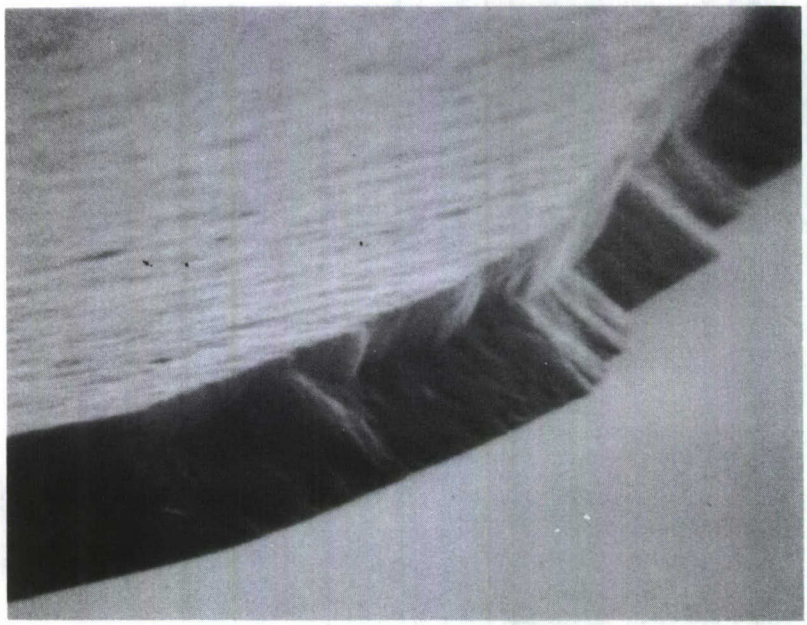


Figure 25. SEM of SOS Island Edge Etched in 6N KOH + CH_3OH, Run 101D

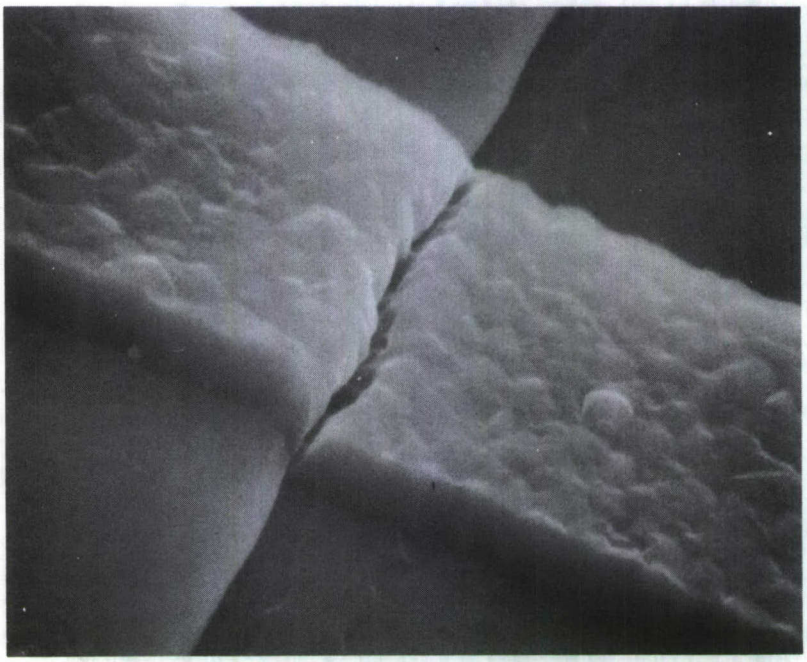


Figure 26. SEM of Open Aluminum Metal at an Island Edge, Run 101B

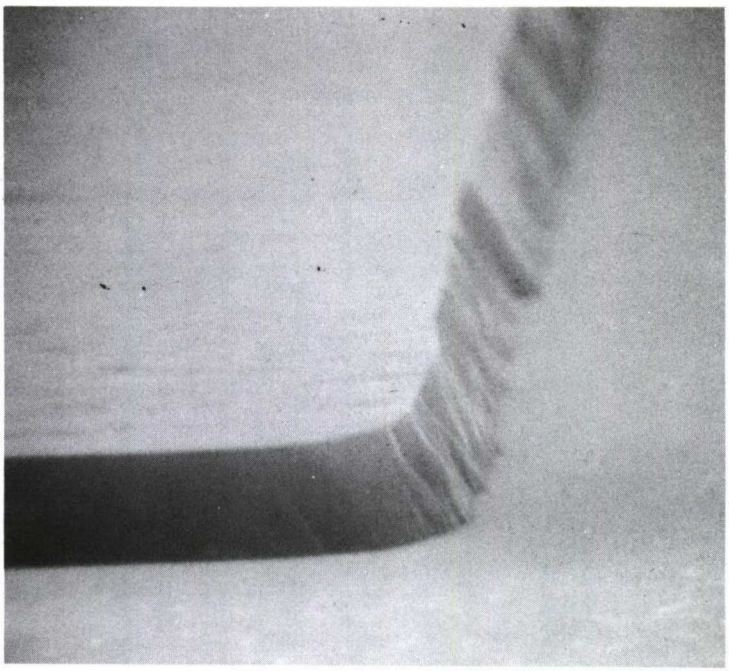


Figure 27. SEM of SOS Island Edge Etched in 6N KOH + Isopropyl Alcohol, Run 106

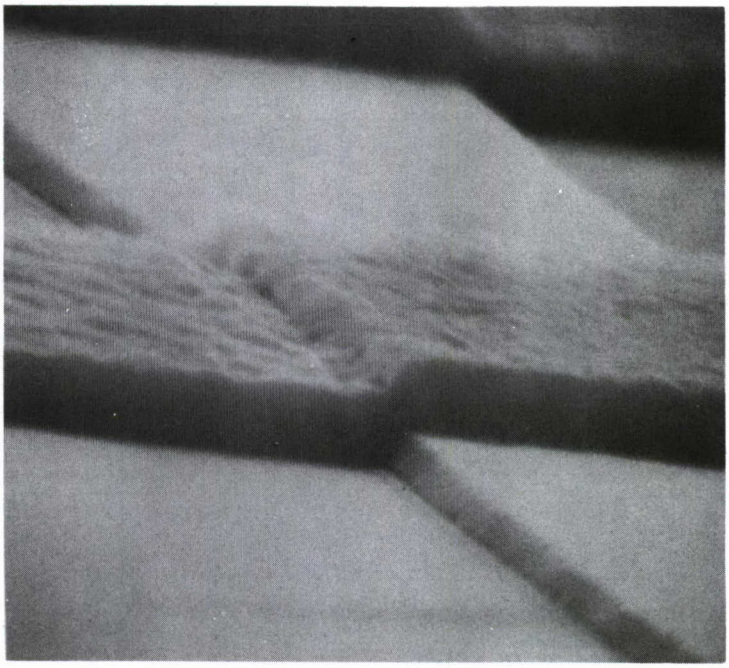


Figure 28. SEM Showing Excellent Aluminum Metal Step Coverage at a Tapered Island Edge, Run 106

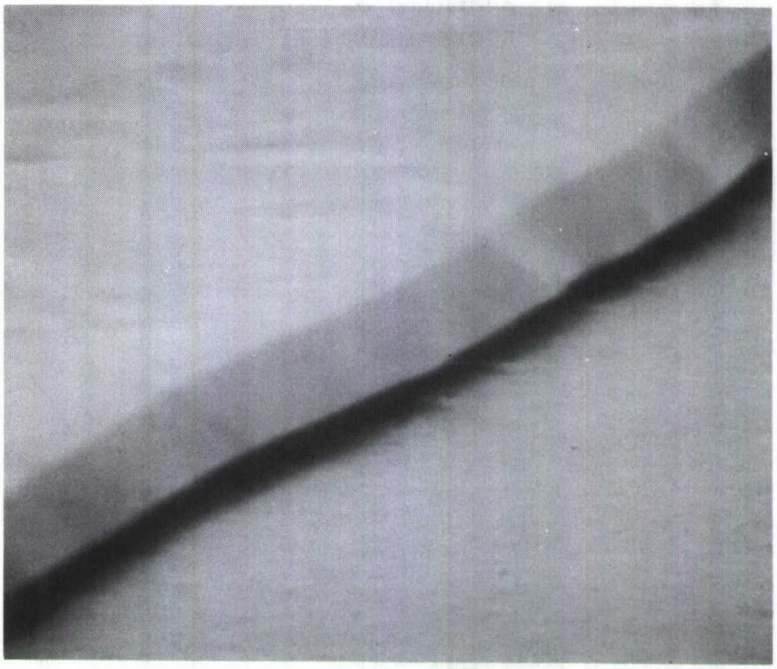


Figure 29. SEM of N^+ Region After Drive in an Oxidizing Atmosphere, Run 110

been possible to obtain diodes operating in the normal manner. Unfortunately, increasing the diffusion time also increases the chances for gaps to occur between the N^+ and P^+ oxides and sapphire. An example of this in Figure 27 is an N^+ oxide showing that a gap at the sapphire interface. Such gaps result in open metal step coverage. Consequently, the P^+ and N^+ masks were modified such that only those regions requiring P^+ or N^+ were defined. With these changes and taking special care during the deglazing operation after phosphorus predeposition the yield of good diode switches and protection devices increased significantly to the point where a finite overall circuit yield could be achieved.

The diode bridge switch circuits contain resistors which were designed for a nominal value of 20KΩ or 9.7Ω/ . These resistors are formed at the same time as the P-wells. Early experiments indicated that a dose of $8x10^{12}$ cm^{-2} at 200KEV gave approximately the desired resistance and source drain breakdowns and thresholds for the N-channel devices. However, the resistor values have varied from about 3-8KΩ/ . The reasons for the low sheet resistances are not clearly understood. Since low valued resistors in the diode switch circuit degrade circuit performance experiments have been carried out to adjust the low valued resistors upward by counterdoping with ^{31}P at a fixed energy of 180 KEV and various doses. After implant the resistors were annealed at 480 deg C in nitrogen for 30 minutes. After anneal the resistors were measured on a type 576 curve tracer. The V-I curves were linear for low ^{31}P doses up to currents of about 1 milliampere, then became nonlinear at larger currents. At higher doses the V-I curve becomes nonlinear at much lower currents (~100μamp or less). The resistance was measured over the linear portion of the V-I curve, and the dependence of resistance on ^{31}P dose is shown in Figure 28. At a fixed energy of 180 KEV Figure 30 shows that a dose of $3x10^{12}$ cm^{-2} gives the desired resistance of 20KΩ or 8.7KΩ/ .

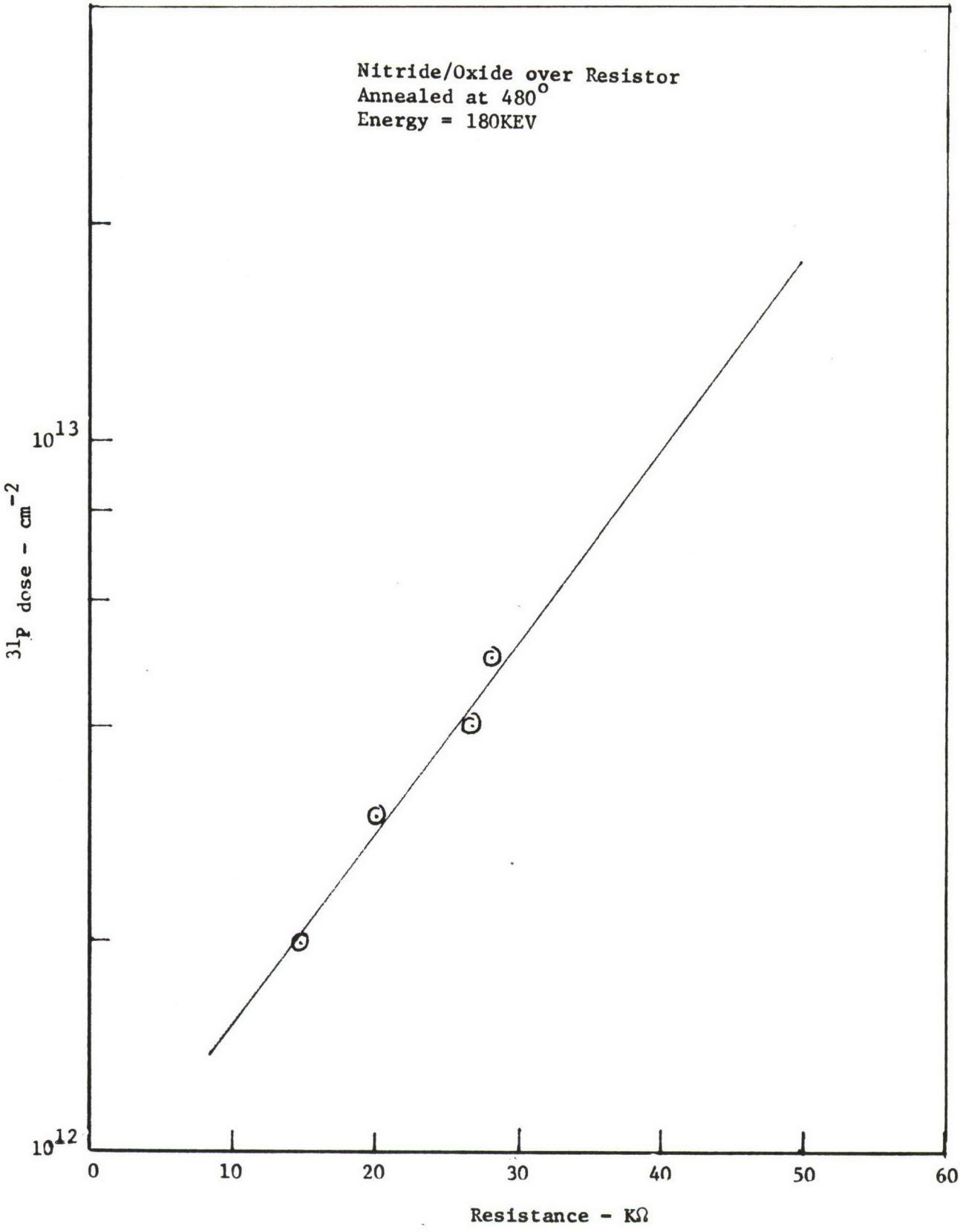


Figure 30. Resistor Adjusting Implant

After modifying and revising the gate, P^+ and N^+ masks, the taking great care during the various processing steps, a significant increase in yield has been achieved. In lot 124A (4 wafers) the yield of perfect circuits before scribing was 22, 25, 29 and 31 percent respectively.

Test Device Characteristics

In each STDL-4 chip there are test devices which can be probe tested. Typical test device results obtained on a number of completed wafers are listed in Table 1. Figure 31 a, b and c shows typical gain characteristics and thresholds of N and P channel MOSFET's as well as the source drain breakdown curve of an NMOS device.

A 2 in. diameter silicon on sapphire wafer containing 160 CMOS integrated circuits is shown in Figure 32. An enlarged view of an individual circuit is shown in Figure 33.

Table 1. Test Device Characteristics

Device	Typical Values	Design Values
Special resistor (diode switch resistor)	7,000-20,000 ohms	15,000
P^+ resistor (P channel source-drain diffusion)	150-200 ohms per square	150 ohme per square
N^+ resistor (N channel source-drain and cross under diffusion)	30-40 ohms per square	30 ohms per square
P^+N^+ diode, V_B at 5μamp	5.5 volts	6.0 volts
Protection diode V_B at 5μamp	22 volts	24.0 volts
PMOS (0.3x0.5 mil)		
V_{th} at 0.5μamp	1.2-2 volts	2 volts
BV_{DSS}	35-40 volts	15 volts
I_{DSS} at -10v	3-10 nanoamp	<1,000 nanoamp
μ_{FE}	220 cm^2/vsec	220 cm^2/vsec
NMOS (0.3x0.5 mil)		
V_{th} at 0.5μamp	1.5-3 volts	2 volts
BV_{DSS}	16-20 volts	15 volts
I_{DSS} at 10v	3-3000 nanoamp	<5,000 nanoamp
μ_{FE}	290 cm^2/vsec	290 cm^2/vsec

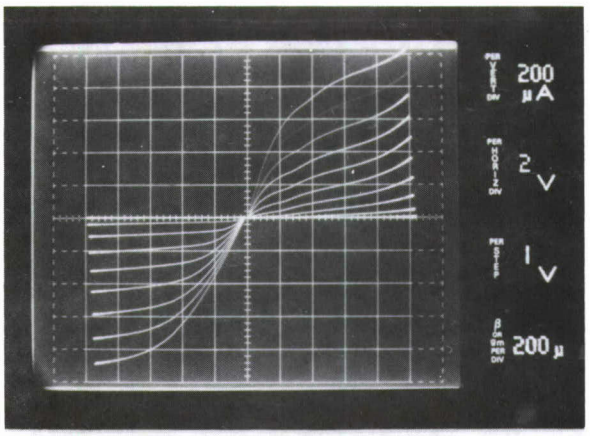


Figure 31(a). Gain Characteristics of N and P Channel MOS (0.3x0.5 mil)

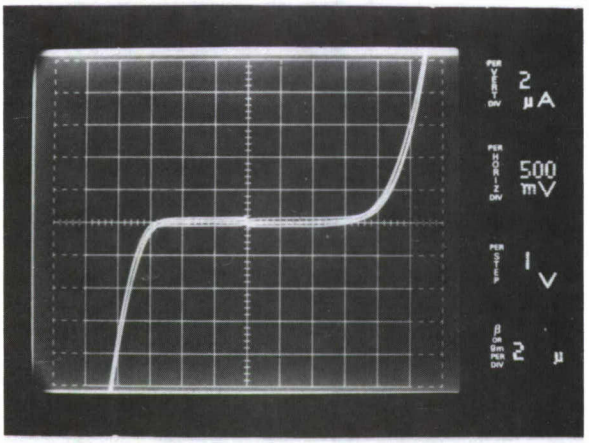


Figure 31(b). Threshold Curve of N and P Channel MOS (0.3x0.5 mil)

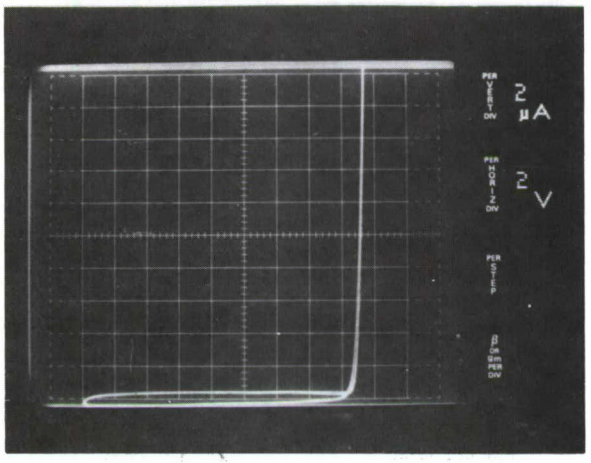


Figure 31(c). Source Drain Breakdown of N Channel MOS (0.3x0.5 mil)

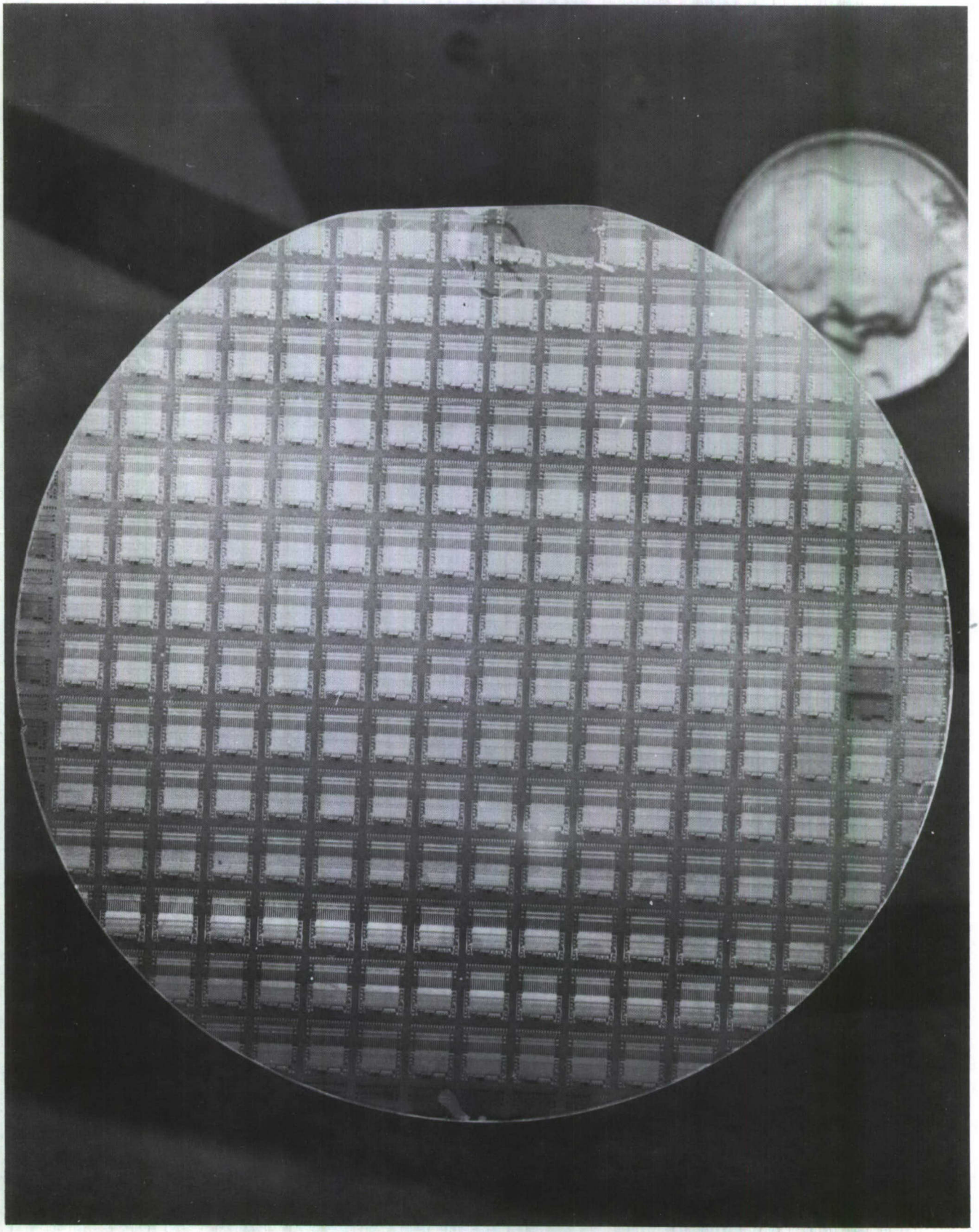


Figure 32. CMOS/SOS Integrated Control Circuits on 2 In. Diameter Sapphire Substrate

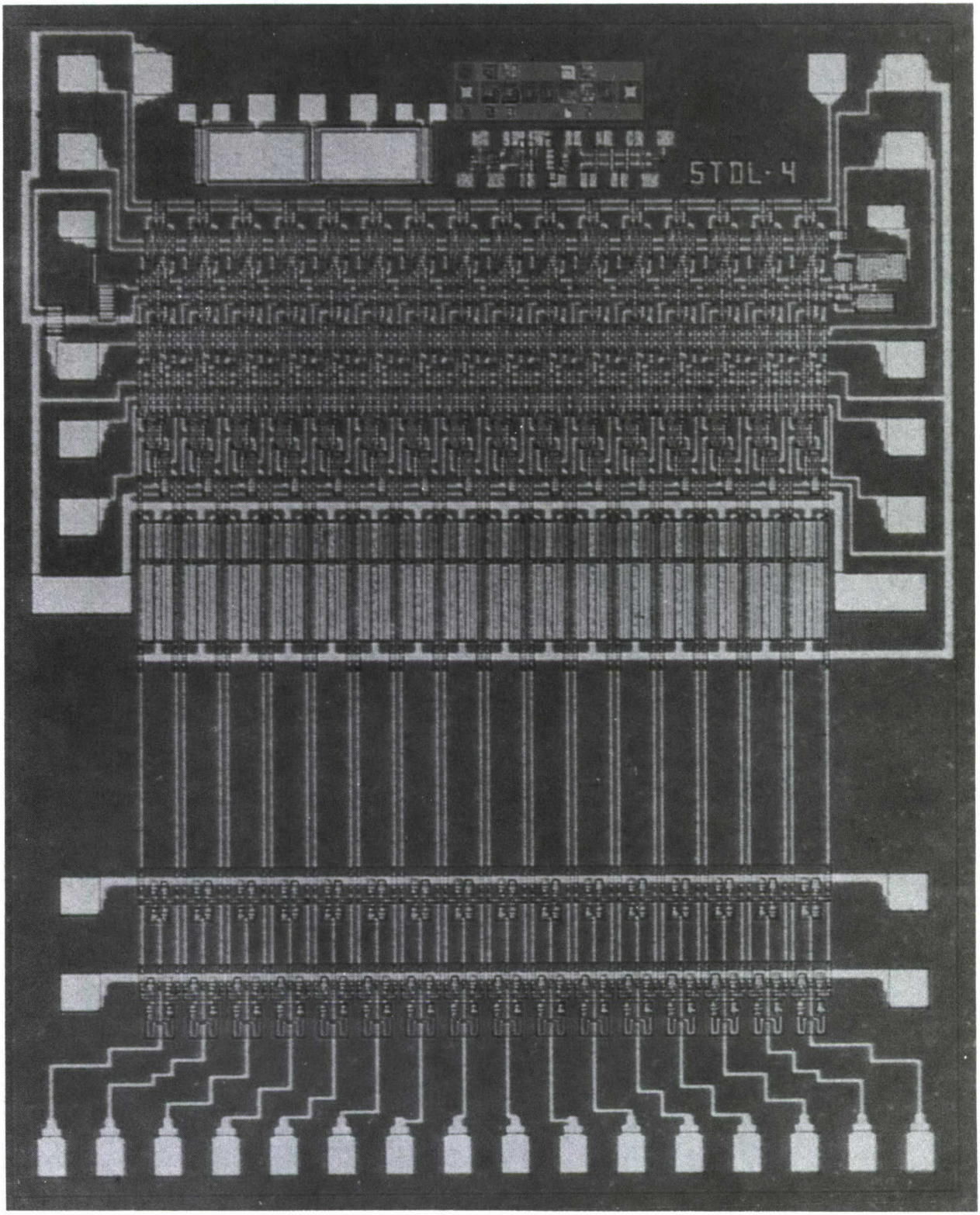


Figure 33. 16 Tap Control Circuit (70X)

Circuit Speed

Typical power dissipation vs clock frequency for the CMOS/SOS circuits developed on this program is shown in Figure 34. For these tests, the switch drivers were disconnected so that the power dissipation at low frequencies, 10^5 Hz and lower, would be only that of the leakage currents in the transistors, primarily the NMOS devices. The upper frequency end of each curve represents the maximum operating frequency at the given power supply level that satisfactory data transfer was achieved, the exception being those curves for V_{DD} = +12V and +15V where the testing circuitry became nonfunctional before the tap switching integrated circuit. At the selected supply level of +10 volts, the upper clocking frequency limit is 35 MHz, well in excess of the 13 MHz required by this program.

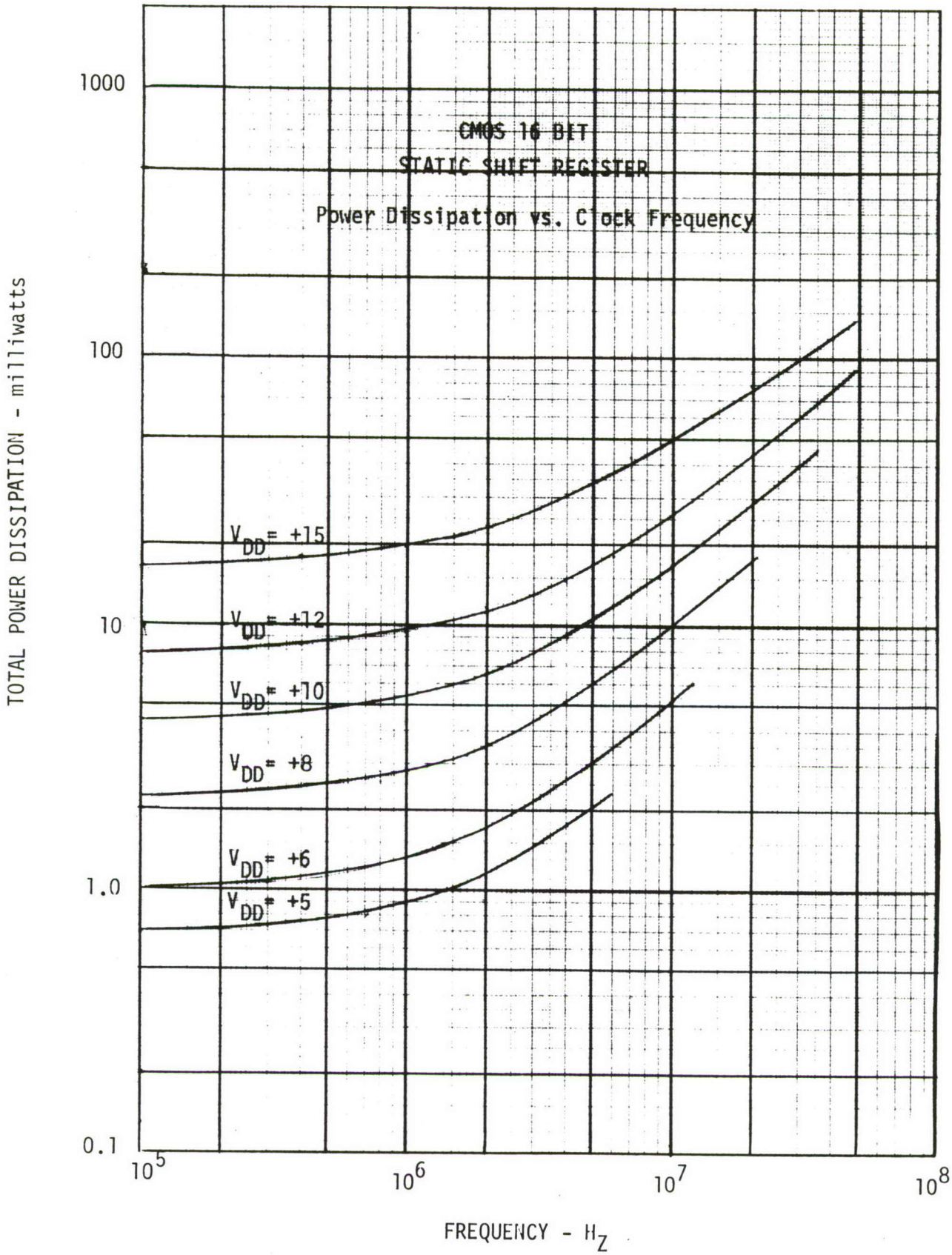


Figure 34. Typical Power Dissipation vs Clock Frequency for the CMOS/SOS Circuits

3.4 INTEGRATED PROGRAMMABLE TAPPED DELAY LINE ASSEMBLY

3.4.1 PTDL Integrated Package

The acoustic TDL of Section 3.2 along with the tap control circuitry of Section 3.3 results in the integrated PTDL shown in Figure 35. The lower portion of the figure shows the integrated assembly with its lid removed. Here the input circuit is on the right with a single toroidal inductor used for series tuning. To the right of the inductor is a metal partition used to reduce direct RF feedthrough. At the bottom of the package are the control circuit input lines for programming input. In the center region are contained the tap control circuits which were discussed in previous sections. At the left side is shown the balanced summing transformer connected to the control circuit sum lines and finally to the output connector. The upper portion of Figure 35 shows the completed PTDL with lid in place ready for operation.

The programmable delay line, Figure 35, is encased in a package milled from aluminum. It is 4 inches long (including SMA RF connectors) 15/16 in. high and 7/16 in. wide. A 15 pin card edge connector protrudes from one edge. With the package placed cover up and card edge connector at the bottom, the control inputs are from right to left:

1. N/C
2. Ground
3. Clock
4. Data Input
5. V+ (10 v)
6. Clock
7. N/C
8. N/C
9. V+ (10 v)
10. N/C
11. Data Output (Test Point)
12. Transfer
13. Transfer
14. Ground
15. V+/2

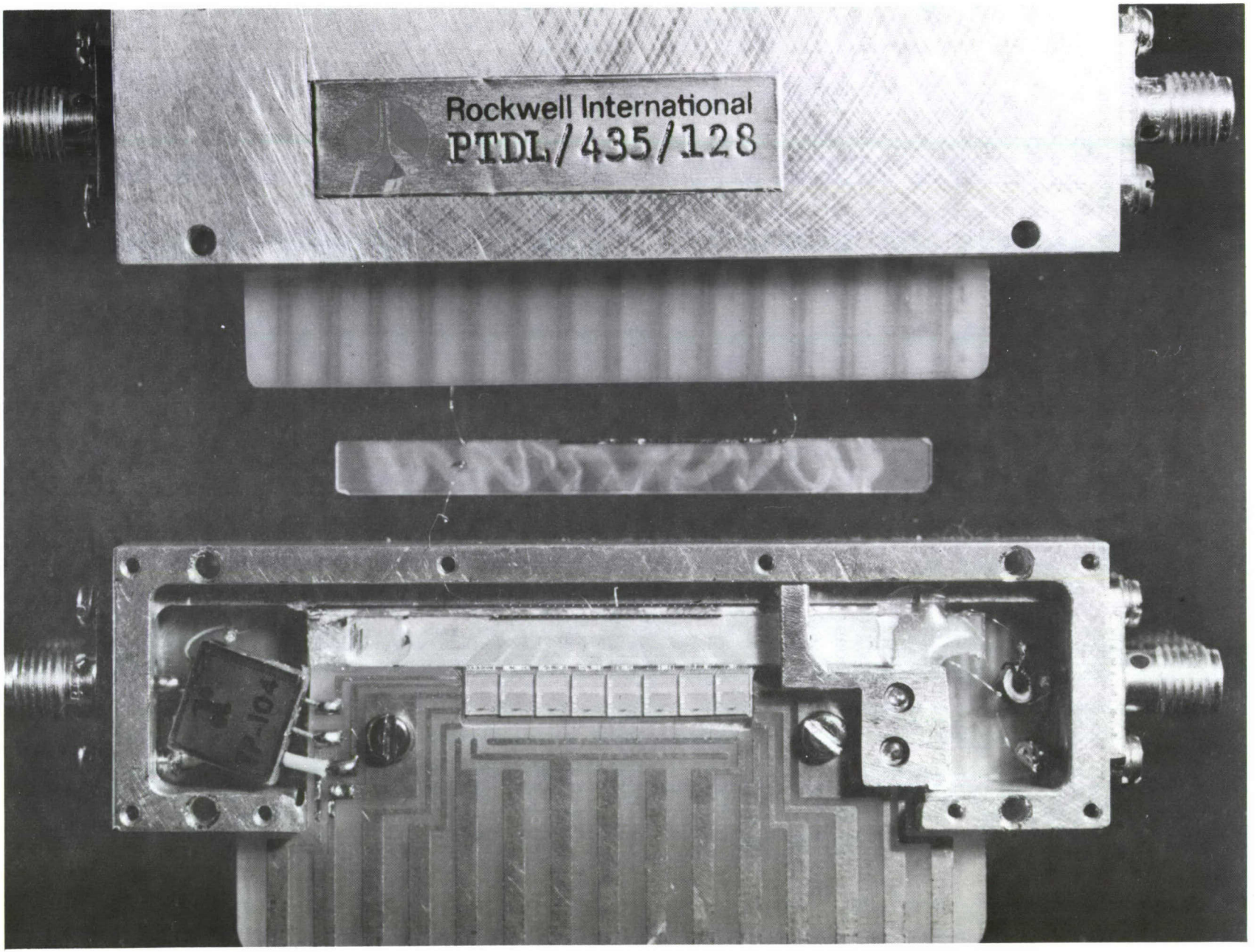


Figure 35. 435 MHz PTDL (Integrated Package Configuration)

And the RF inputs are:

	Right	Left
PTDL-435/20/128-C (Correlator)	Input	Output
PTDL-435/20/128-M (Modulator)	Output	Input

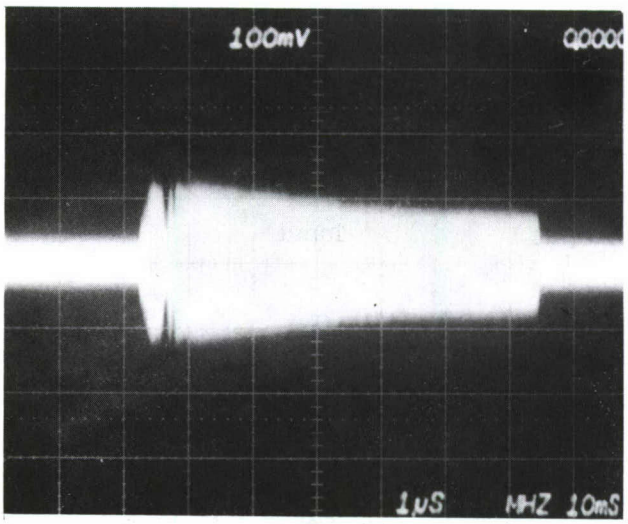
3.4.2 PTDL Experimental Results

The 435 MHz PTDL's developed on this contract were evaluated by several techniques. First, an impulse response evaluation was carried out with the codes set for all "0" or all "1" to check for inoperative taps and amplitude variations. Any asymmetry in the two sum lines also shows up in this response as shown in Figure 36(a) and (b). This PTDL had four bad taps as can be seen in the response. An unexpected roll-off of 5 to 6 dB down the line was obtained instead of the uniform response expected based on the response of Figure 21. Also, differences between the "0" and "1" sum lines as a function of position down the lines were noted.

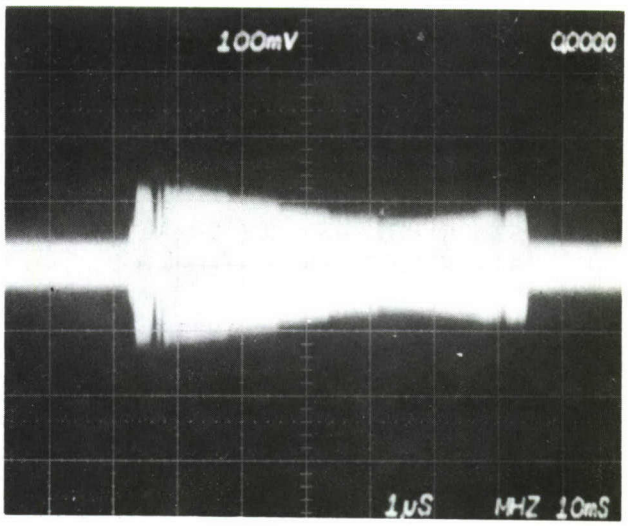
Second, the all "0" and all "1" correlations were checked with an externally generated RF tone burst having a time extent equal to that of the whole tap array. Deviations from a perfect triangular envelope on a normal oscilloscope time domain presentation indicates either tap amplitude variations, phase deviations, or both. Figure 36 (c) and (d) show the results. The frequency was adjusted on this test to give the closest possible approach to perfect triangulation to determine the center frequency for both the "0" and "1" case. For the case shown f_o("0") = 435.157 MHz and f_o ("1") = 435.136 MHz to give a 21 kHz difference. This difference indicates phase differences between a given tap's contribution to the total current delivered to the load depends on whether the tap is connected to one sum line or the other. A slight difference between the two sum lines was expected since one line sees a little more capacitance to ground than the other due to crossover capacitances in the integrated circuit. The observed difference however is significantly larger than would be expected from simple lumped element circuit analysis.

Further device evaluation included determining the PTDL response for specific coded waveforms generated by standard feedback shift register/double balanced mixer/local oscillator techniques. For this case the input code is nearly perfect and any deviation from theoretically expected performance is due to the PTDL alone. A typical autocorrelation function obtained for a 435 MHz PTDL in this manner is shown in Figure 37 (a). The peak to sidelobe ratio for this and several other PTDLs measured 16 to 18 dB which was 5 to 7 dB less than the theoretical value of 22.99 dB expected for the specific PN code used for this test.

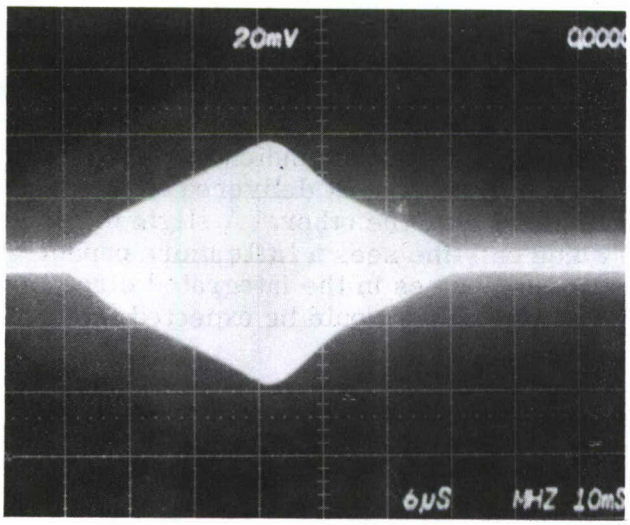
Passive code generation and correlation was evaluated using the two pairs of 435 MHz PTDLs which were incorporated in the two exerciser boxed to be delivered to ECOM. One PTDL of each pair was encoded with the same PN code used for the previous test while the other PTDL was coded with a time-reversed replica of the same code. The waveform generated by impulsing one PTDL was then fed into the other PTDL of the pair with the result shown in Figure 37(b). The peak to sidelobe ratio for this case was typically 12 dB, or 11 dB worse than the perfect theoretical case.



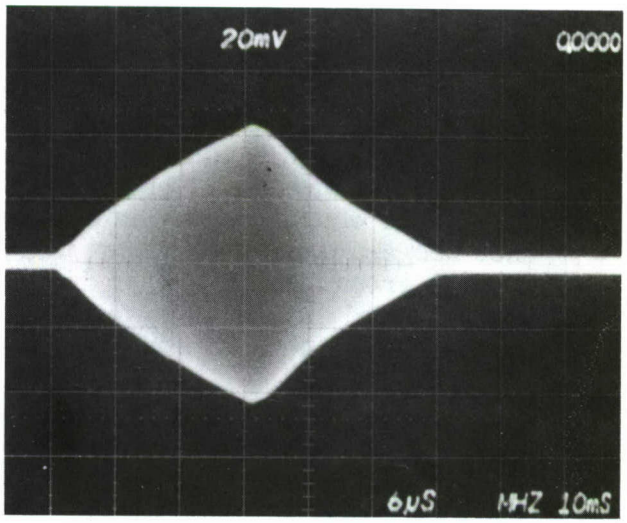
(a) Impulse Response all 1's



(b) Impulse Response all 0's

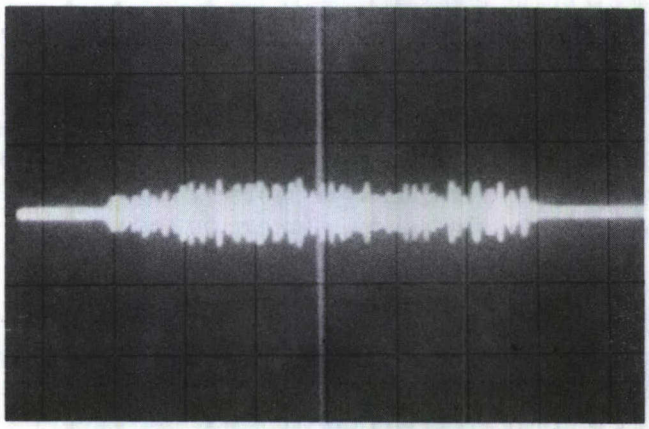


(c) All 0's Correlation

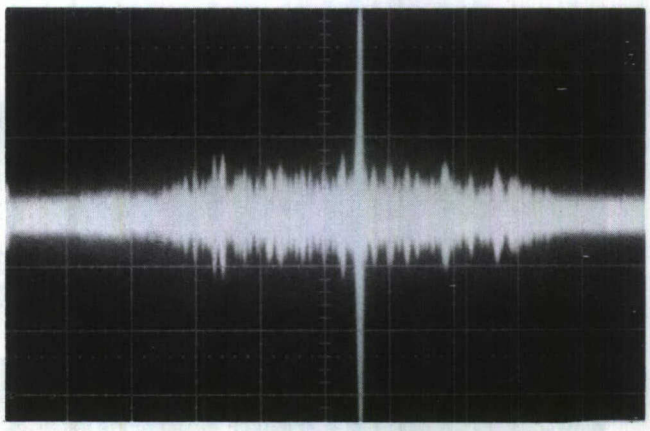


(d) All 1's Correlation

Figure 36. Typical 435 MHz PTDL Test Results, Scales Defined by CRT Readout are Per Major Division, Both Axes are Linear.



(a) Shift Register Generated Input (Active)



(b) PTDL Generated Input (Passive)

Figure 37. PTDL PN Code Correlation Results. (100 mv/cm Vertical, 2 μsec/cm Horizontal)

Insertion loss from input spread waveform to correlation peak was measured for all PTDLs fabricated and results fell between 51 dB and 55 dB. This corresponds to 93 dB to 97 dB loss from input to a single tap. These values are significantly higher than the corresponding 42 dB and 84 dB figures expected from the analysis described in Section 2.4.

The discrepancies between theory and experiment for the 435 MHz PTDLs were obviously due to the relatively high center frequency since 70 MHz PTDLs designed and fabricated at Rockwell International on other programs have shown much superior performance. Figure 38, for example, shows the autocorrelation function of a 70 MHz PTDL for the same PN code used for the 435 MHz device. Peak to sidelobe ratio at 70 MHz was 22 dB - less than 1 dB worse than the 22.99 dB maximum obtainable peak to sidelobe ratio for this code. Insertion loss was within 2 dB of theoretical.

A new frequency-dependent model was therefore required which would account for the observed discrepancies. Symptoms apparent from the experimental data on the 435 MHz lines such as impulse response roll-off, differences between "0" and "1" sum lines, and insertion loss discrepancies, indicated the signal sum lines in the integrated circuits were acting as lossy loaded transmission lines.

The sum lines were therefore modeled as periodically loaded transmission lines as described in detail in the next section. Good agreement was obtained between performance predictions based on this model and the experimental results, and design changes necessary to significantly improve device performance on subsequent devices can now be identified.

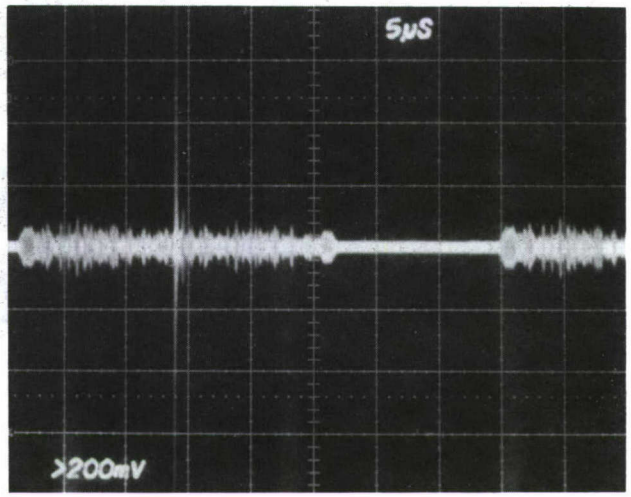


Figure 38. PTDL Correlation Performance at 70 MHz

3.5 TRANSMISSION LINE MODELING OF PTDL TAP CIRCUITS

3.5.1 Introduction

This section describes in detail the transmission line model developed to resolve the discrepancy between predicted and measured PTDL characteristics. The influence of these transmission line effects on device performance as a function of velocity errors (due to either crystal orientation errors or doppler frequency shifts) is also examined with respect to both peak to sidelobe ratios for a specific 127 chip PN maximal length sequency and insertion loss. The transmission line model basically considers the tap switching circuits as adding shunt capacitance and resistance to the transmission sum lines which increases the effective electrical length of the sum lines to approximately 2.4 radians/inch at 435 MHz. Since the discrete shunt loading is uniformly distributed over the sum line length and also constitutes many elements per electrical degree, the line is treated as if the loading were in fact continuous. When this assumption is made, the analysis proceeds in a straightforward manner. The analysis is presented here in three parts, first the general analysis assuming known transmission line parameters, second a breakdown of the tap switching circuits into useful transmission line parameters, and third a number of computed results are presented wherein tap circuit parameters are varied.

3.5.2 General Transmission Line Modeling

The following analysis applies to the case of a single active tap driving the sum line. The sum line is represented by a transmission line made up of shunt and series elements which includes the other inactive taps. The modeling thus applies to the impulse response configuration wherein the taps are active one at a time in sequency as the surface wave propagates along the delay line. The active tap is modeled as a current source, I, shown in Figure 39 located a distance X_1 from the first tap or beginning of the sum line and X_2 from the last tap, or end of the sum line. The total length of the sum line is X_1+X_2 and is a constant. The current I from the tap splits and flows to the left toward the open end of the sum line and also toward the load R_L. The quantity of interest is the voltage E_L produced across the load resistance R_L. Transmission line equations may now be used to determine E_L in the following manner. First the voltage at the tap position is given by

$$E_t = IZ \tag{1}$$

where

$$Z = \frac{Z_1 Z_2}{Z_1 + Z_2} \tag{2}$$

Here Z_1 is the impedance of the open circuit transformed through a length of line X_1,

$$Z_1 = Z_o \frac{\cosh \theta_1}{\sinh \theta_1} \tag{3}$$

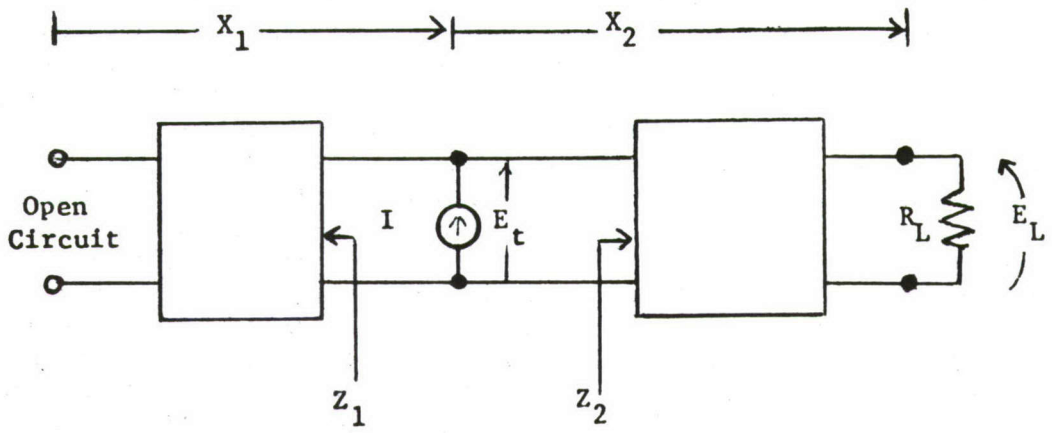


Figure 39. Transmission Line Model of Parallel Sum Lines

and similarly Z_2 is the transformed load impedance

$$Z_2 = Z_o \frac{R_L \cosh \theta_2 + Z_o \sinh \theta_2}{Z_o \cosh \theta_2 + R_L \sinh \theta_2} . \tag{4}$$

Here the transmission line parameters are

$$\theta_1 = \gamma X_1$$

$$\theta_2 = \gamma X_2$$

$$= \sqrt{R+j\omega L} \quad \sqrt{G+j\omega C} \qquad \text{Propagation Constant} \tag{5}$$

$$Z_o = \sqrt{R+j\omega L} \; / \; \sqrt{G+j\omega C} \qquad \text{Characteristic Impedance} \tag{6}$$

where ω = radian frequency

R = series resistance, per unit length

L = series inductance, per unit length

G = shunt conductance, per unit length

C = shunt capacitance, per unit length .

Once E_t is determined, the voltage at the load is given by

$$E_L = E_T \frac{R_L}{R_L \cosh \theta_2 + Z_o \sinh \theta_2} . \tag{7}$$

It is useful to normalize E_L by the voltage $R_L I$ which would be produced if there were no transmission line effects or tap switching circuits, i. e., each tap would independently see the same load. The normalized amplitude is then defined by

$$A = \frac{E_L}{R_L I} \tag{8}$$

and may be found in general from by substituting (3) and (4) into (2) to find E_t in (1) and then (1) into (7) to find E_L and finally substituting (7) into (8). The result is

$$A = \frac{z_o \cosh \theta_1}{[\cosh \theta_2 + z_o \sinh \theta_2] \sinh \theta_1 + [z_o \cosh \theta_2 + \sinh \theta_2] \cosh \theta_1} \tag{9}$$

where $z_o = Z_o/R_L$

Note that in general z_o, θ_1, and θ_2 are all complex functions when the line is assumed to be completely general.

If the line length shrinks to zero, then A is unity. But as $\omega \to 0$ A is less than unity because

$$\gamma(\omega = 0) = \sqrt{RG}$$

and $Z_o(\omega = 0) = \sqrt{R/G}$

are finite and correspond to a lossy capacitor in shunt with the load.

3.5.3 Transmission Line Parameters

The required transmission line parameters to be used in (9) are R, L, C, G. Here R is simply determined by the resistance per unit length of the Aℓ metalization stripe which forms the sum line in the circuit package and has a value of 5-10 ohm/cm. In the absence of switching circuits, the two sum lines can be modeled as low loss parallel balanced lines having characteristic impedance Z' which is known. Thus, the equivalent capacitance and inductance are given by

$$C' = \frac{\sqrt{\epsilon}}{V_c Z'} \tag{10a}$$

$$L' = \frac{Z'\sqrt{\epsilon}}{V_c} \tag{10b}$$

where V_c = volocity of light

ϵ = effective permittivity

Z' = characteristic impedance

L' = series inductance/unit length

C' = shunt capacitance/unit length .

The modeling assumes that this basic transmission line is uniformly loaded by shunt elements due to the taps and associated switching circuits. Since only shunt loading occurs, R is as given and L = L'. It is now only necessary to determine the effect of the shunt loading. The circuit shown in Figure 40(a) represents a case where one set of diodes are forward biased, resistors R_d, and the other set is reverse biased, capacitances C_d corresponding to ON and OFF states respectively. The tap is given its parallel equivalent circuit represented by I_a, G_a, C_T and the bias resistors, R_b, are tied to RF ground. The cross-over capacitance is given by C_c such that if the cross-over is to the + sum line than $C'_c = C_c$ and $C''_c = 0$, and when the cross-over is to the - sum line than $C'_c = 0$ and $C''_c = C_c$. In this manner the slight asymmetry between + and - sum lines can be accounted for. Because of the symmetry in the diode rings, the circuit of Figure 40(a) readily reduces to that of Figure 40(b). The circuit of Figure 40(b) corresponds to a balanced transmission line which is fed "off center" and is therefore relatively difficult to analyze compared to a more simple model to be employed here. First note that the diode forward resistances are small compared to other circuit impedances (even at 435 MHz) and are accordingly replaced by short circuits. If this is done, then C'_c has no effect and so is also set to zero. Now, the reactances of capacitors $2C_d$ are not necessarily much larger or much smaller than the associated resistance $R_b/2$.

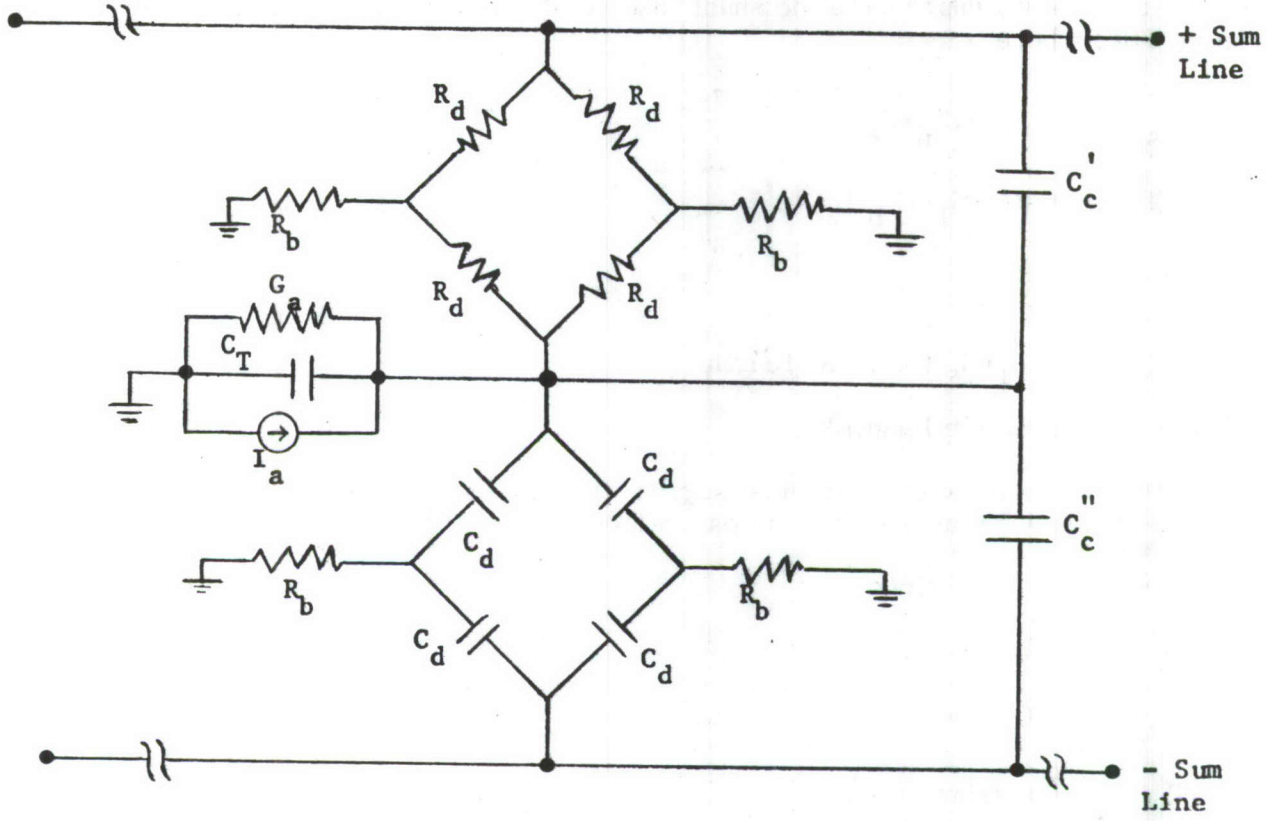
Rather than handle the circuit as two parallel transmission lines, as is required by the unbalanced drive, a reasonable assumption is to take the -sum line at ground potential since the current flows mostly into the + sum line. When this is done, the circuit reduces to that of Figure 41(a) where

$$G'_b = G_b \frac{Q^2}{1+4Q^2} \tag{11a}$$

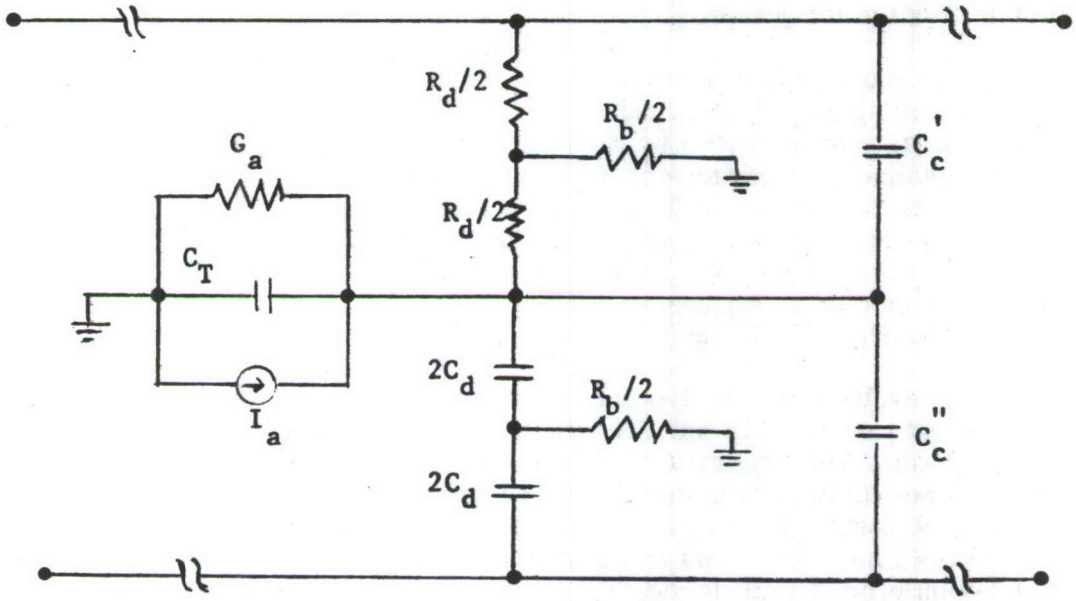
$$C'_d = 2C_d \frac{1+2Q^2}{1+4Q^2} \tag{11b}$$

$$Q = \omega C_d R_b \tag{11c}$$

$$G_b = 2/R_b \tag{11d}$$



(a) Tap Switch Circuits



(b) Electrical Equivalent of(a)

Figure 40. Switching Circuit Models

Thus, Figure 41(a) represents the shunt loading of the transmission line as shown in Figure 41(b) where

$$C_s = (C_T + C'_d + C_c)L \tag{12a}$$

$$G = (G_a + G_b + G'_b)L \tag{12b}$$

where $L = \frac{N}{X}$

$X = X_1 + X_2$ total line length

and N = No. of taps in length X .

The factor L is used to convert the discrete loading to a continuous "per unit length" loading. The new transmission line parameters are now given by

R = R, as given

L = L' from (10)

$C = C' + C_s$

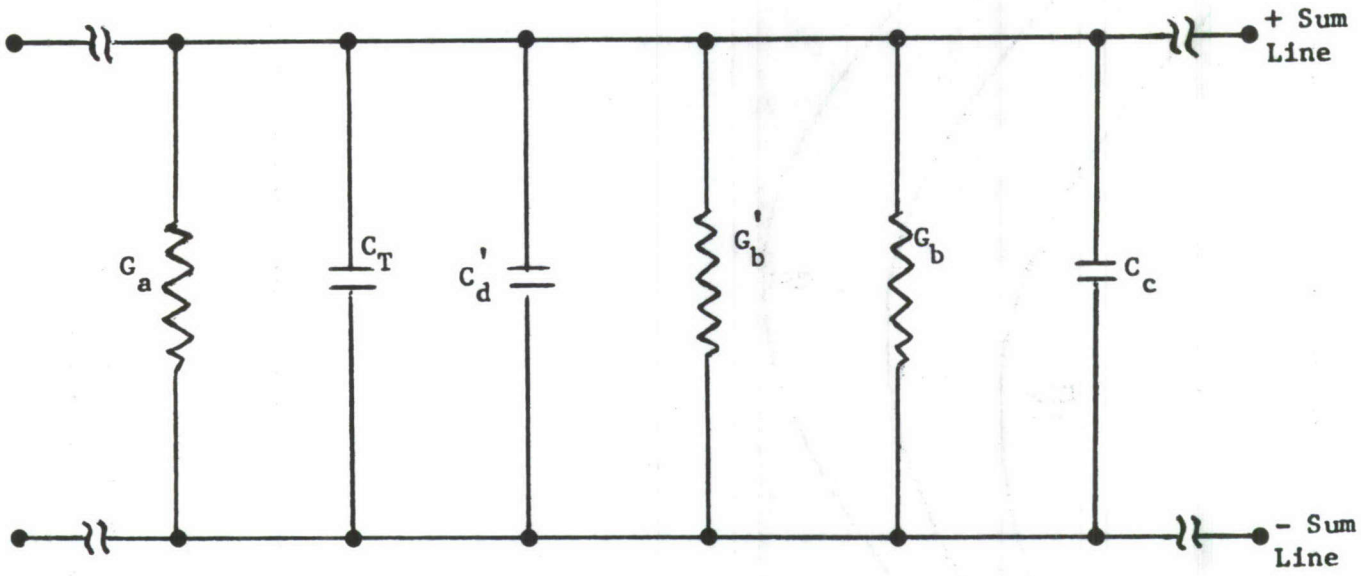
G = G from (12)

which may be used to find Z_o and γ for the transmission line.

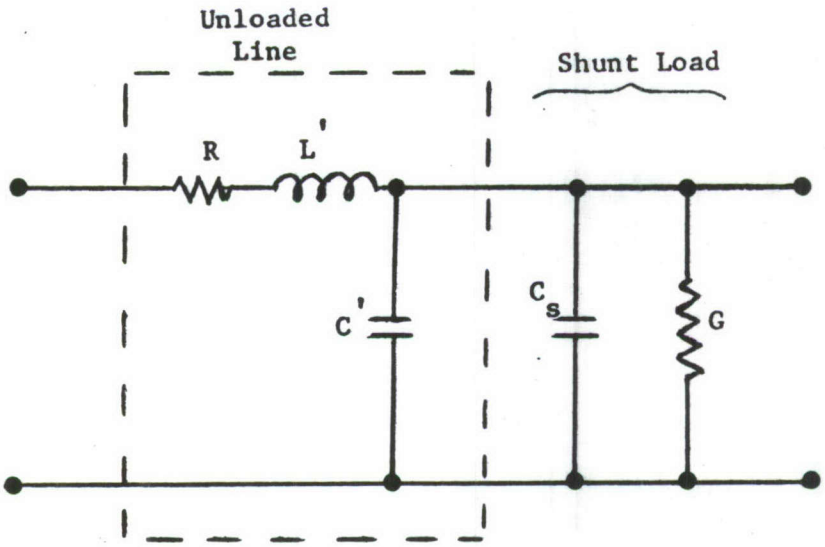
3.5.4 Calculated Impulse Response

Using the above equations, a number of cases having different circuit parameters were calculated using the HP 9830 calculator. These results have the output load amplitude normalized to that produced by the first tap. The results in Figure 42 have the series loss resistance as a parameter showing the cases R = 0, 5, and 10 ohm/cm with all other parameters as given in Table 2. Note that a value of 200Ω is used for the load resistance because in the actual device the 50Ω load is connected to the transmission lines via a center-tapped 2:1 transformer. Figure 43 has R_b as a parameter (in K ohms) with R=5 ohm/cm. Figure 44 has the diode off capacitance (in pf) as a parameter for the case R_b = 12.5K and R=5 ohm/cm.

The computed results show the typical response observed experimentally, the amplitude is largest at the first tap and decreases for taps nearer the load, then increases near the load. The explanation of this response is as follows: At the first tap the load resistance has been transformed to a larger value and hence E_t is larger because of the current source drive. But as the position of the driven tap is shifted toward the load, this impedance drops and also more current begins to flow to the left. The transformed open circuit impedance, Z_1, drops as X_1 increases reaching a minimum where the imaginary part of θ_1 is equal to 90 deg. When the active tap approached the load, the current begins to favor the load side whose impedance is decreasing relative to the impedance transformed from the left which is increasing. The response is quite sensitive to the circuit parameters since the line is very lossy



(a) Shunt Loading Elements



(b) Shunt Load Added to Unloaded Transmission Line Segment

Figure 41. Transmission Line Shunt Loading

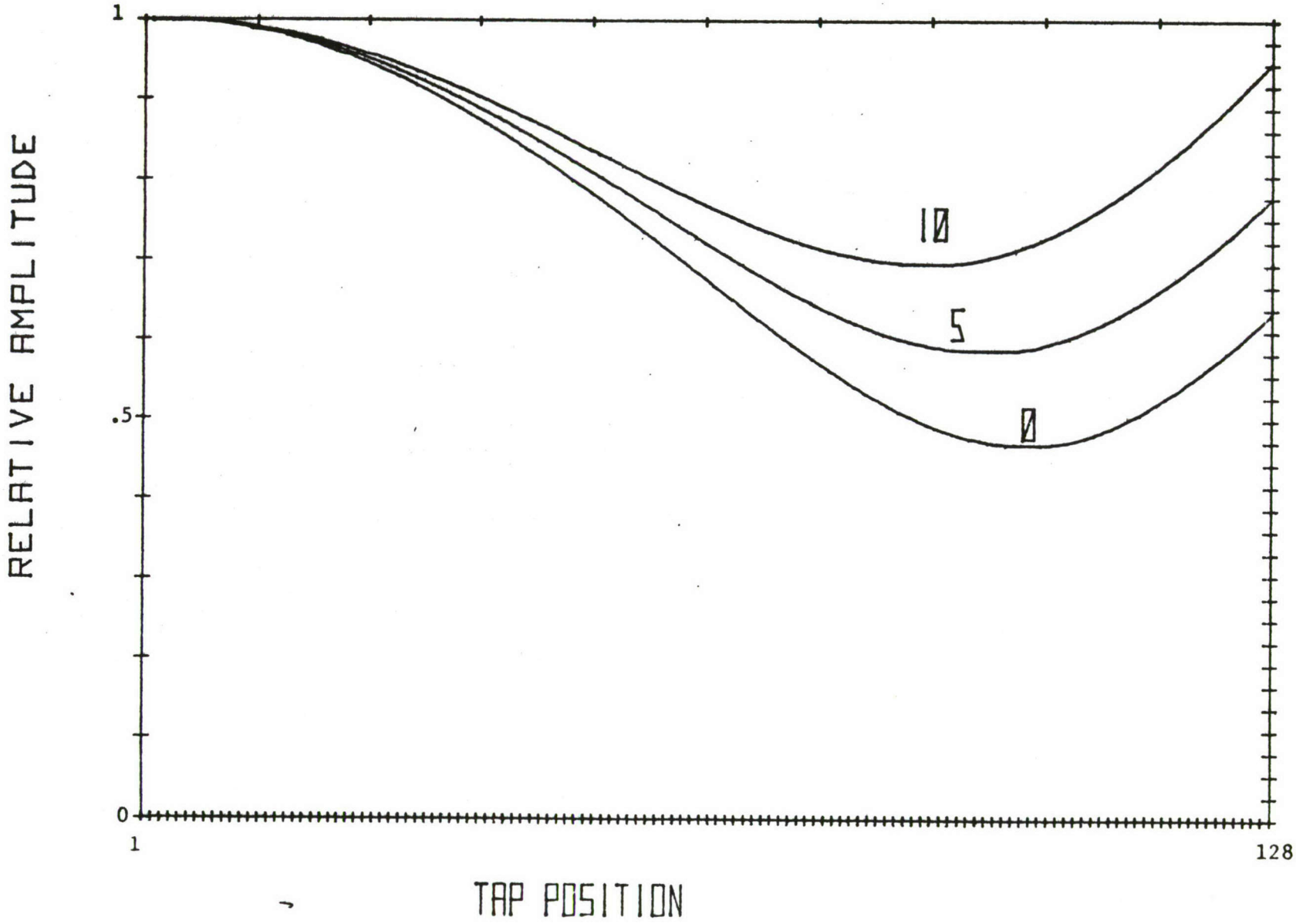


Figure 42. Tap Amplitude, Normalized to the First Tap as a Function of Tap Position with Series Loss, R, in Ohms per cm as a Parameter

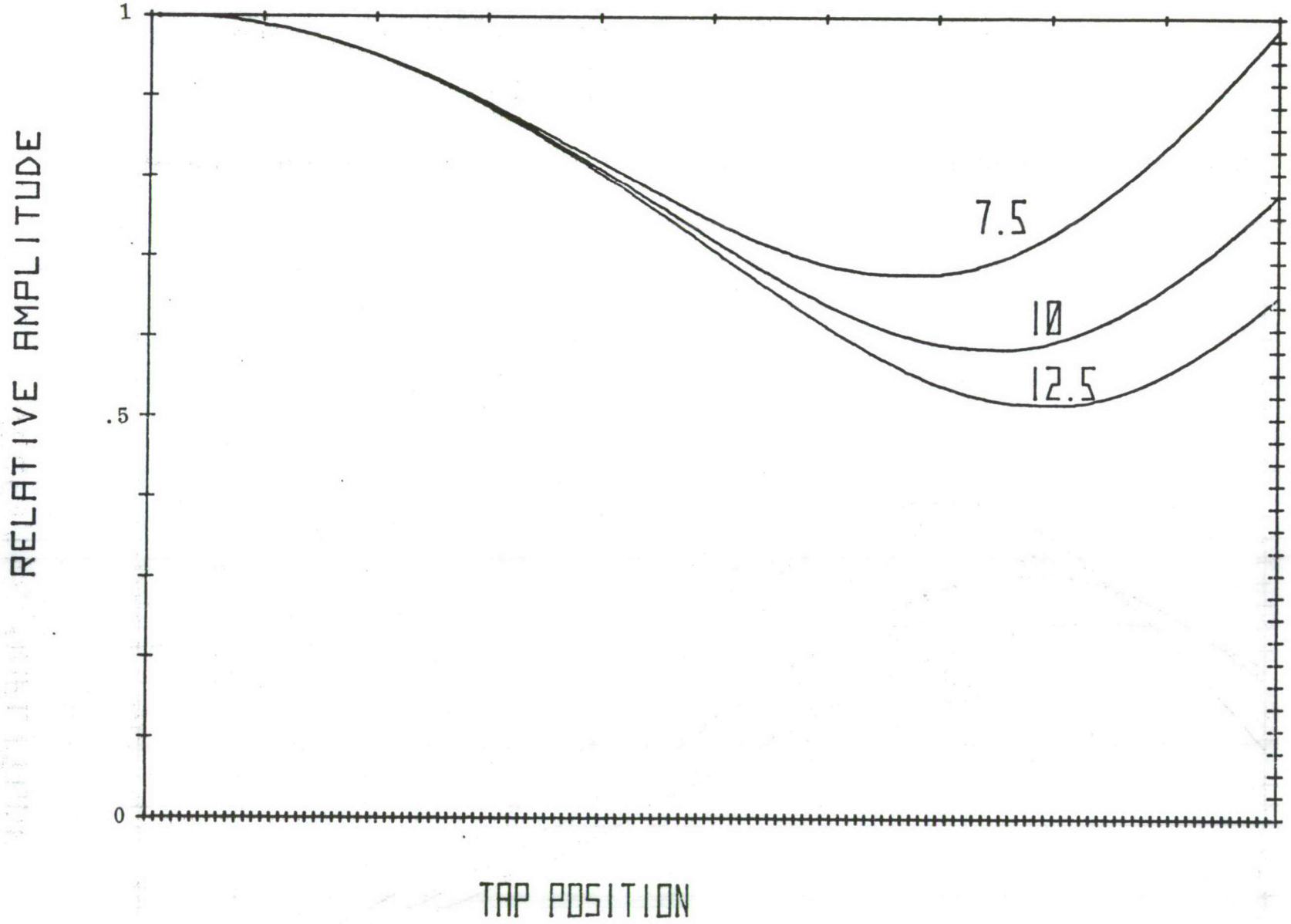


Figure 43. Tap Amplitude as in Figure 42 Except R=5 ohm/cm and R_b, Bias Resistor in K ohms is the Parameter

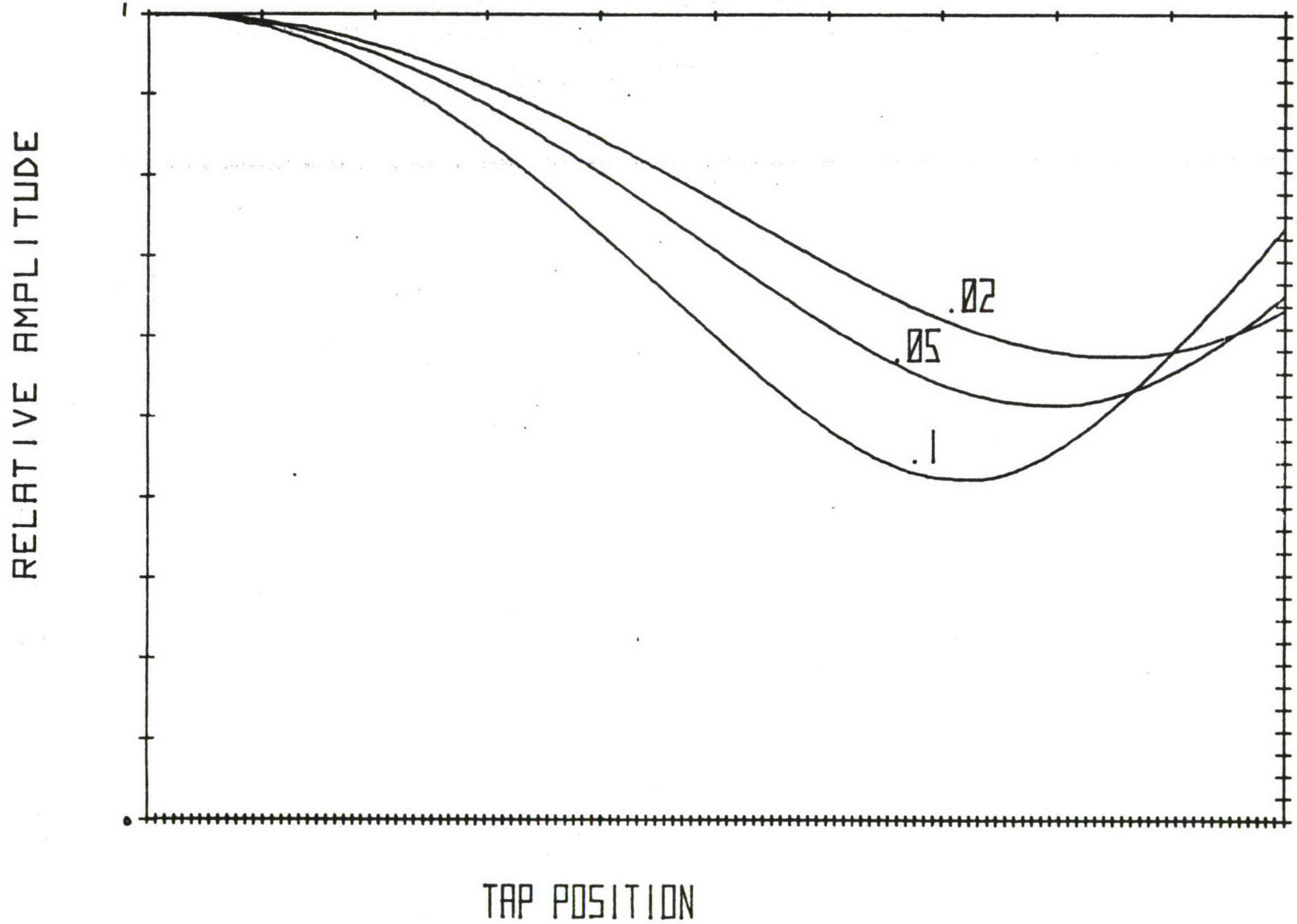


Figure 44. Tap Amplitude as in Figure 43 Except R_b=12.5 K ohms and C_d, Diode Off Capacitance in pf is the Parameter

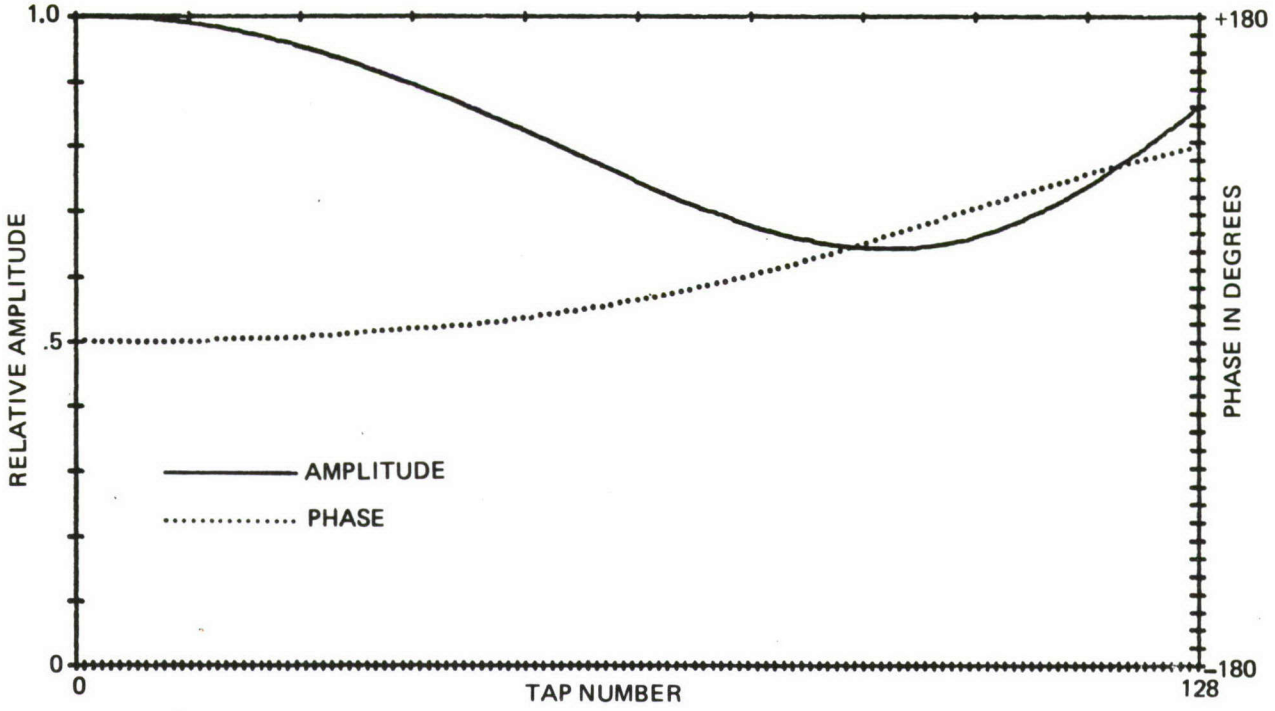
Table 2. Circuit Parameters Used for Transmission Line Modeling of Tap Circuits and Sum Lines

Z'	=	150 ohms
ϵ	=	6
C_T	=	0.05 pf
C_c	=	0.02 pf
C_d	=	0.05 pf
R_b	=	10 K ohms
f	=	435 MHz
N	=	128 taps
X	=	0.76 in., line length
R_L	=	200 ohms

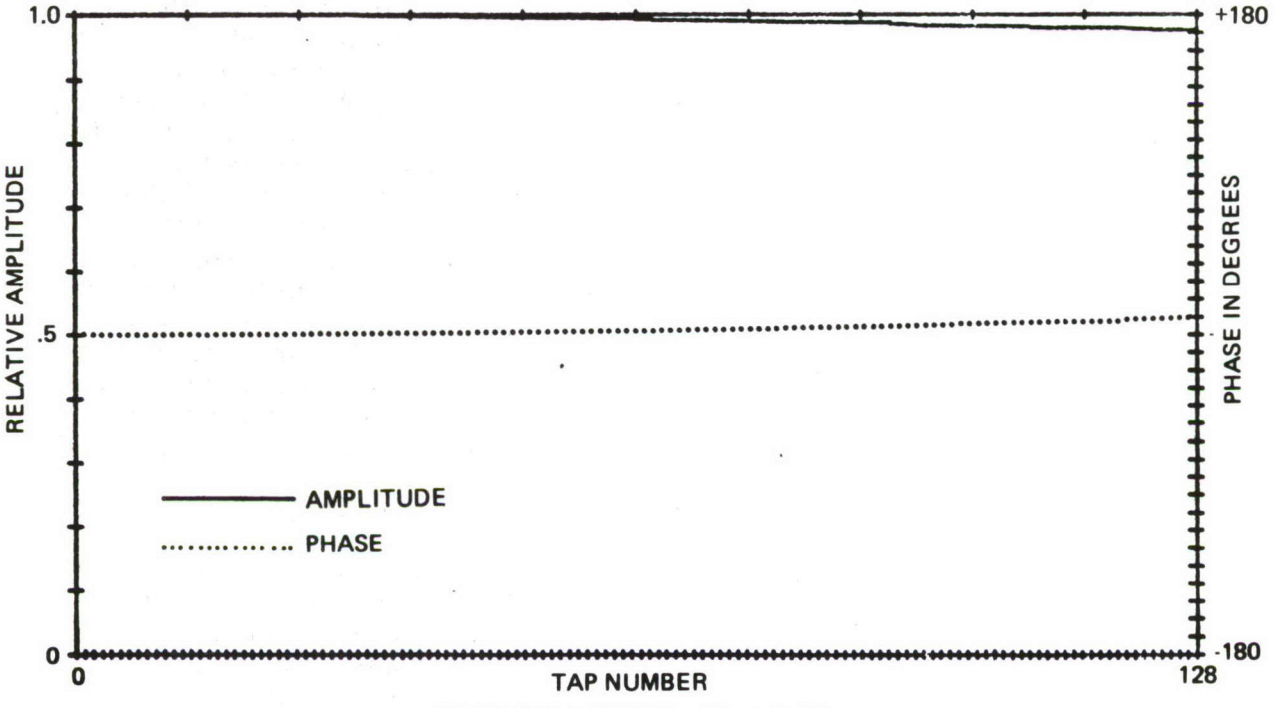
making γ sensitive to real and imaginary shunt impedances. Typical calculated results of important circuit parameters are given in Table 3 for the case R=5 of Figure 42. Here it is readily apparent that the line is very lossy and that the characteristic impedance is complex. Note that C is much larger than C' indicating that the shunt loading capacitance largely determines the transmission line parameters. The output signal due to an input from the first tap is given by A_1 = -17 dB where A_1 has been normalized to the output obtained by a single tap in the absence of any other taps or transmission line effects. Thus the 17 dB insertion loss represents the additional loss due to the transmission line composed of other taps and switch elements. The best fit to the experimental results for the all "0" device is given in Figure 42 and Table 2 for R $\approx$ 7.5 ohm/cm. The plot for this case is shown in Figure 45(a). Here the phase is also calculated and indicates a significant departure from linearity. The nonlinearity in phase response gives rise to a degradation in correlation peak-to-sidelobe ratio. Shown in Figure 45(b) is the same case as above except for operation at 70 MHz and shows a slight (.25 dB) roll-off in amplitude and very little (<10 deg) phase nonlinearity which explain the excellent autocorrelation performance with 22 dB peak-to-sidelobe ratio observed experimentally. (Figure 38).

3.5.5 Autocorrelation Predictions for the Transmission Line Model

The previous section described the transmission line model and predicted an increase in insertion loss to the first tap from the 84 dB of the lumped circuit analysis analysis (Section 2.2) to 72 dB+17 dB = 89 dB. Since the tap output amplitudes are not uniform and tap outputs do not add in perfect coherence, due to phase deviations, it is no longer valid to consider device insertion loss from spread waveform to the correlation peak to be equal to the insertion loss of a single tap less 20 Log_{10}(N) where N is the number of taps.



(a) 435 MHz PTDL, IL = 17 dB



(b) 70 MHz PTDL, IL = 6 dB

Figure 45. Tap Output Amplitude and Phase

Table 3. Calculated Transmission Line Parameters

γ	=	0.9 + j 2.4 per in.
Z_0	=	33 + j 7.4 ohms
C'	=	1.4 pf/in.
L'	=	31 nh/in.
C	=	23 pf/in.
R_P	=	24 ohms
A_1	=	-17 dB

A model was therefore set up which calculated autocorrelation performance and insertion loss increase for a 127 chip maximal length code of 2667 wavelengths extent taking into account the amplitude and phase deviations of Figure 45(a). Three separate cases were calculated. Case A assumes a perfect 127 chip maximal length PN code (actively generated) incident on an actual 127 tap 435 MHz PTDL which has the impulse response of Figure 45(a) and considers the effect of errors (in parts per million) on performance. These errors can be due to either doppler frequency shifts, quartz orientation errors, or temperature effects, all of which cause a further loss in coherent tap addition. Case B is for the passive code generation case where an imperfect waveform is generated by impulsing one 435 MHz PTDL and correlating this waveform with another 435 MHz PTDL where both PTDLs have the impulse response of Figure 45(a). Case C is for the ideal case of a perfect waveform correlated in a 435 MHz PTDL which has uniform amplitude tap outputs and zero phase deviations.

The results of this analysis are shown in Figure 46(a) and (b). Extra insertion loss in Figure 46(b) is defined as 20 Log_{10} ($127A_1/A_p$) where A_1 is the amplitude of the signal from the first tap, determined from an impulse test, and A_p is the amplitude of the correlation peak.

Theoretical peak/sidelobe ratio for Case A at 0 ppm error is 18.7 dB. This corresponds to the case of Figure 37(a) and is close to the 16 - 18 dB peak/sidelobe ratios obtained experimentally on the six 435 MHz PTDLs under case A conditions. The small discrepancy remaining (.7 - 2.7 dB) can be explained by considering missing taps. For example, consider a 127 chip PN code which has a maximum sidelobe of 15. The peak to sidelobe ratio is therefore 127/15 = 8.5 or 18.6 dB. Now say 5 taps are missing from a delay line in which this code is correlated and the 5 taps all correspond to a "1" tap setting then the maximum sidelobe will probably increase from 15 to 20 giving a peak/sidelobe ratio of 127/20 = 6.35 or 16.1 dB. The device processing gain ($10\text{Log}_{10}N$ where N is the number of taps) is however reduced by less than .2 dB by the loss of these 5 taps. The number of missing taps on the six 435 MHz PTDLs fabricated on this contract varied from 15 on the first device to 4 on the sixth device as improvements were made in integrated circuit quality and processing and assembly techniques.

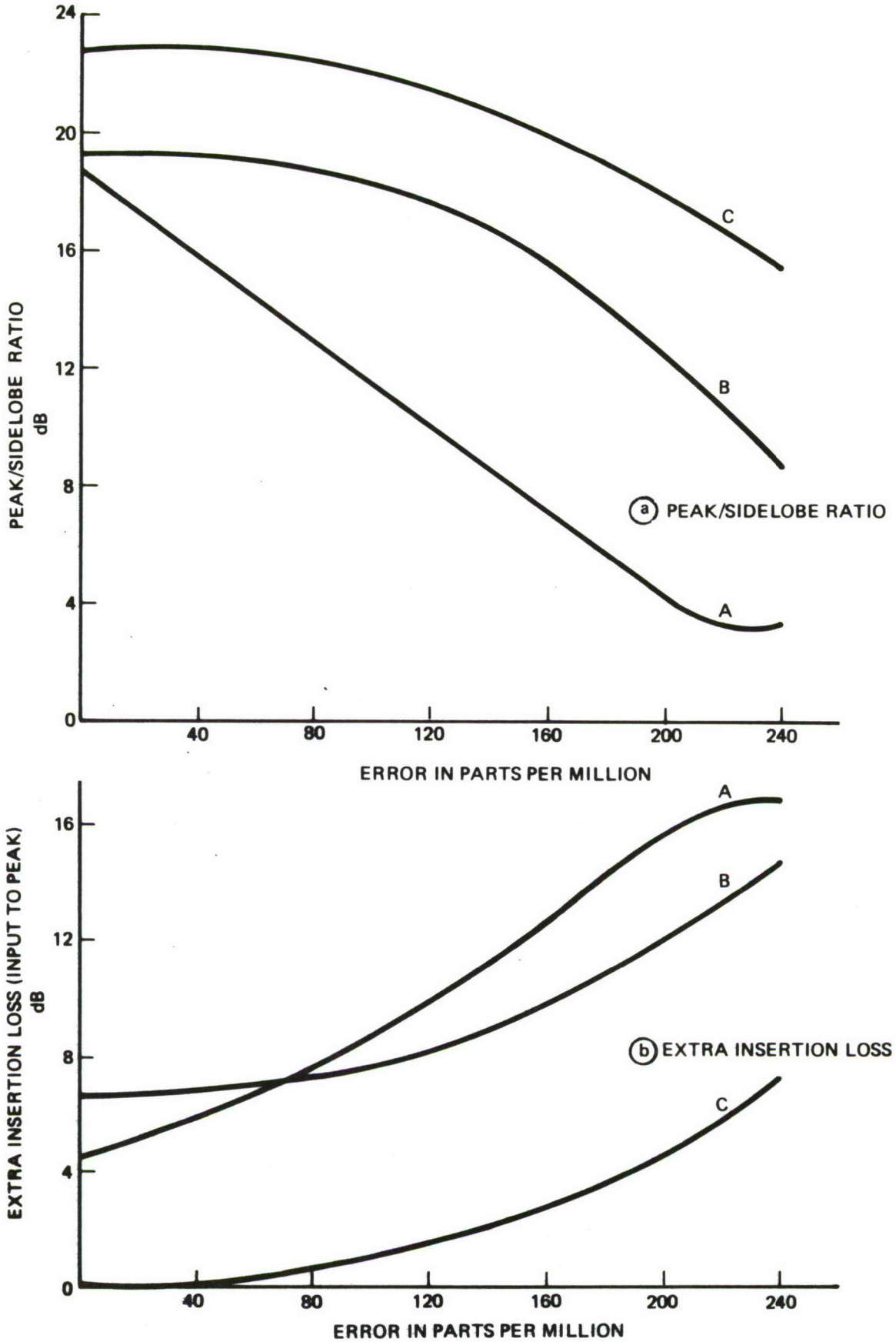


Figure 46. Autocorrelation and Additional Insertion Loss for 127 Chip 435 MHz Waveform with 20.7 MHz Chip Rate

The extra insertion loss for 0 ppm error is 4.5 dB for Case A (Figure 46(b)). This would be expected to result in a net insertion loss, from input spread waveform to correlation peak, of 89 dB - 42 dB + 4.5 dB = 51.5 dB. It can be seen for Curve A (Figure 4.6(b)) an error of 50 ppm would increase the extra insertion loss from 4.5 to 6.8 dB resulting in a new insertion loss of 53.8 dB. These figures agree well with the measured insertion loss spread from 51 dB to 55 dB obtained on the six 435 MHz PTDLs fabricated on this contract.

For Case B the predicted peak to sidelobe ratio does not degrade as rapidly with error as for Case A. This is due to a partial compensation of amplitude and phase errors caused by the time reversed nature of the waveform generator and correlator respectively. Since the generator and correlator are made from different ST quartz bars however significant orientation errors are possible. An orientation difference of +10' for one bar and -10' for the other bar will result in a total error of about 170 ppm (Figure 15) which will reduce the peak to sidelobe ratio to 14.6 dB (Figure 46(a)) and increase the insertion loss by 10 dB (Figure 46(b)). When the influence of a few bad taps on these results is considered then the experimentally measured peak/sidelobe ratio of 12 dB for Case C (Figure 37(b)) is considered within the limits defined by the theory.

Significant improvement in device performance would obviously be obtained if predictions of Figure 45(a) were included in the design. The amplitude variations could readily be compensated for by adjusting the tap overlap weighting while the phase deviations could be compensated for by changing the position of each tap slightly to reduce the relative phase difference between taps to zero. A laser controlled photomask stepping machine would necessarily be required for the photomask since the phase error in Figure 45(a) varies from 0 to 110 deg which corresponds to positional adjustment requirements of zero to 2.2 microns. This does not present a significant problem since several commercial photomask supplies have this capability.

4. 435 MHz TRANSCEIVER

4.1 INTRODUCTION

This section describes the transceiver designed to use the 435 MHz programmable tapped delay lines developed on this contract to demonstrate synchronization and data transmission capability with rapidly changing PN codes and to deliver this equipment to ECOM for further evaluation.

The transceiver is shown in Figure 47. The transceiver specifications are listed in Table 4. Section 4.2 describes the transmitter and receiver design and outlines the operating sequence of the overall transceiver while Section 4.3 presents the experimental data obtained prior to delivery to ECOM.

4.2 TRANSCEIVER DESIGN

System Operation - Transmitter

A system block diagram is shown in Figure 48. The type of data transmission is selected from the front panel. During "Burst" mode data is clocked into a shift register at the highest data rate of 19.2 kHz, but with corresponding redundant data bits. After 16 data bits have been loaded into the shift register, the data is then generated at 312 kHz, differentially encoded and then modulo 2 added to a variable length PN code running at 20.7 MHz. RF modulation is then PSK at 435 MHz. Figure 49 demonstrated the data transmission format while in the burst mode. If a short PN code is selected $(2^{13} - 1) = 8191$. The maximum number of unique bursts allowed before code restart is 7.

$$\left\{ (17 \text{ data bits})^{-1} \times (64 \text{ chip code word})^{-1} \times (8191 \text{ code length}) \right\}$$

The long code is $(2^{23} - 1)$ long and would consequently allow 7,710 bursts before restarting.

The short code was designed for ease of test since code would recycle every 5.8 msec. The long code was designed into the system to increase the amount of anti-jam margin and reduce the spectral density of the basic waveform. Time to recycle is every 6.4 sec.

System Operation - Receiver

A system block diagram is shown in Figure 50. The surface acoustic wave device, also made at the Rockwell International Anaheim R&D facility, has 128 taps controlled by four inputs. See Figure 51. This method was chosen for loading the PTDL because the output of the line is noisy during loading, consequently programmed entry would have to be speeded up in time to accommodate RF data reception (t_p load = 1.6 usec). Programmed entry may be designed to operate in complete parallel access requiring 50 nsec of load time. However, the disadvantage is that this would require at least 128 lines of interface.

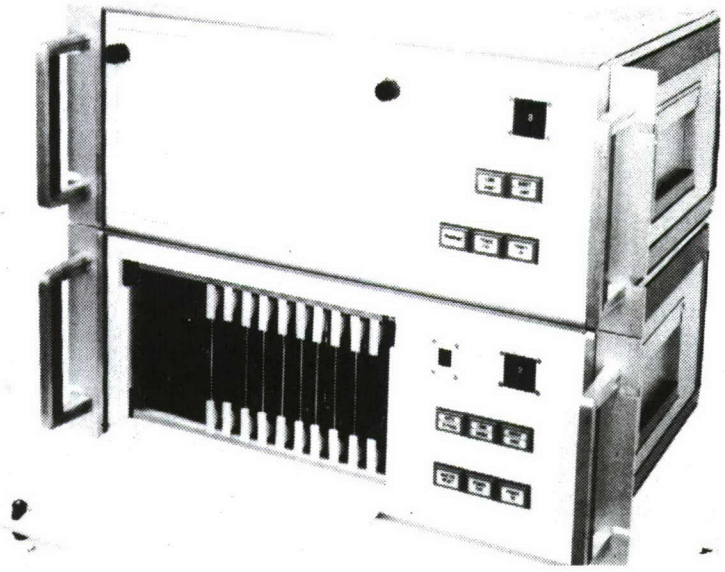


Figure 47. Complete Transceiver

Table 4. Interface Transceiver Specifications

	Transmitter	
Power Output	–	**2 watt (cw.), 3 watt (sat.)**
Carrier Frequency	–	**435 MHz Nominal**
Data Rate	–	**Selectable From Panel as 19.2, 4.8, 2.4, or 1.2 Kbps**
Tx Duty Cycle	–	**Burst Mode = 6.5% Cont. Mode = 100%**
Code Length	–	**Long = 8,388,480 Chips Short = 7,616 Chips**
	Receiver	
Sensitivity	–	**-100 dBm (max) at 16 dB Eb/No**
N.F.	–	**6 dB max**
Surface Acoustic	–	**(2) 435 MHz f_c, Programmable at 20.7 m Chip Rate**
Provides Synch Lock	–	**Short (Burst Mode) = 5.83 ms**
Indication and	–	**Long (Burst Mode) = 6.42 sec**
Acquisition is Within	–	**Short (Cont. Mode) = .36 ms**
Following Limits	-	**Long (Cont. Mode) = .396 sec**

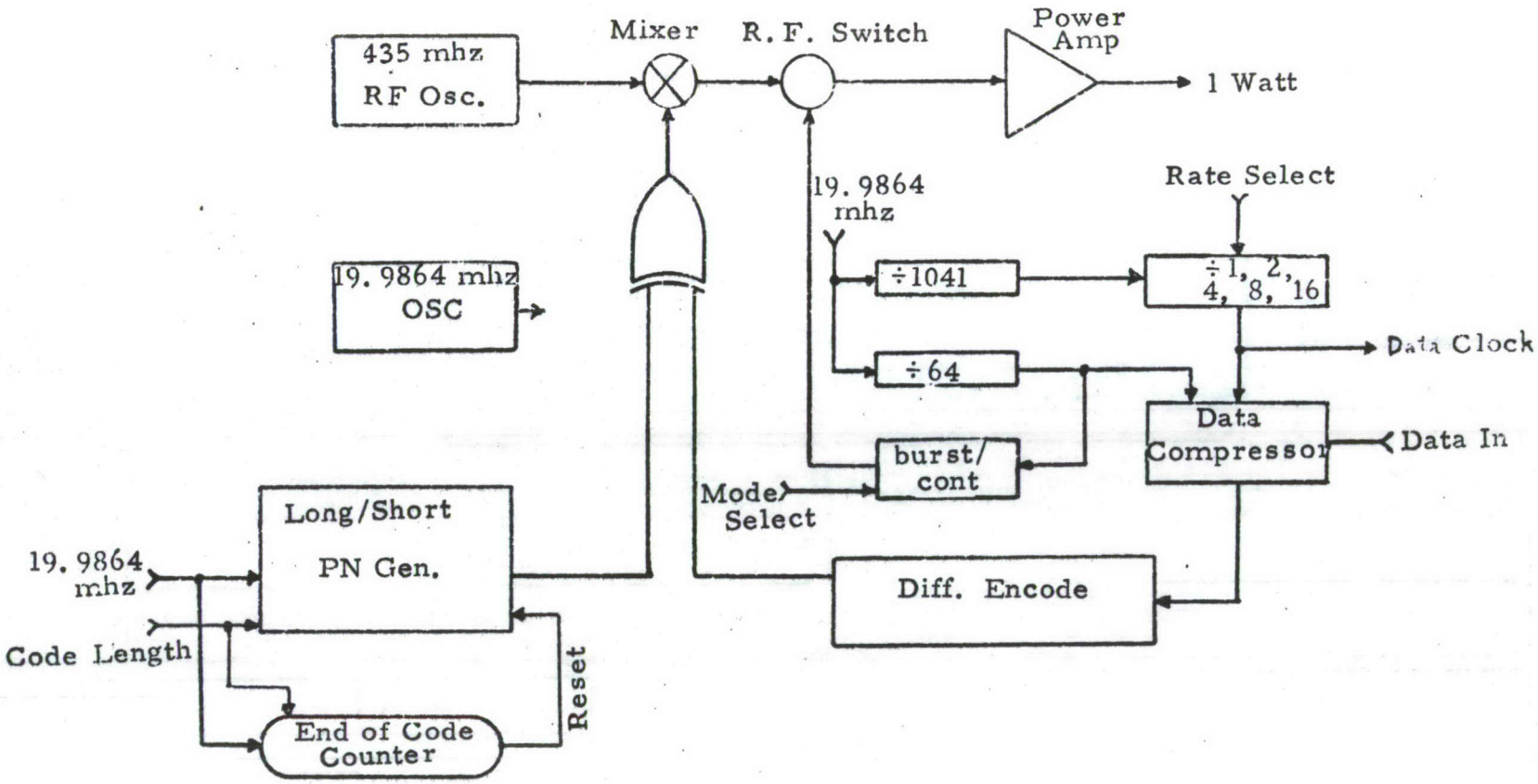


Figure 48. PTDL Interface Transceiver (Transmitter)

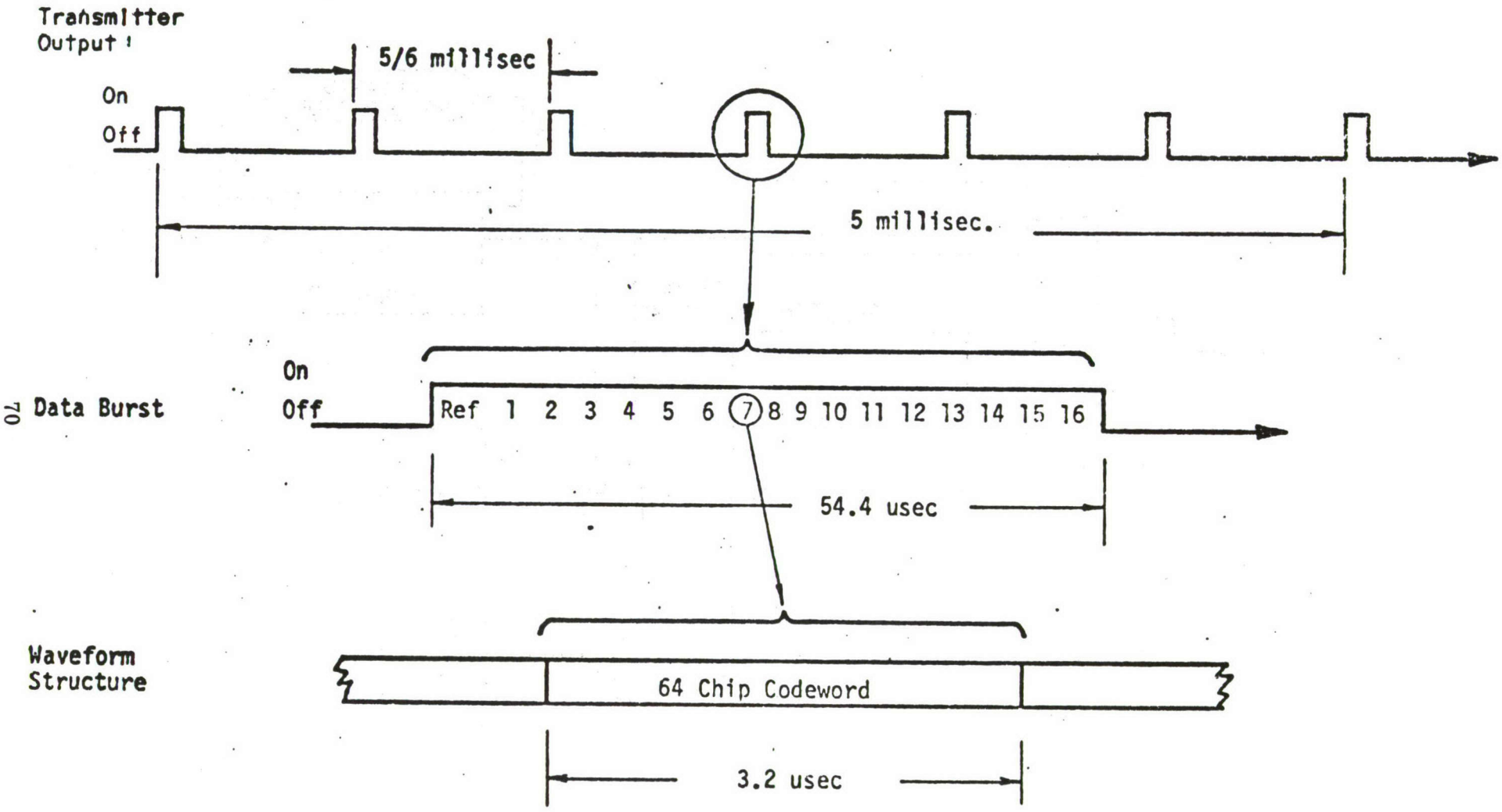


Figure 49. Burst Data Transmission Format

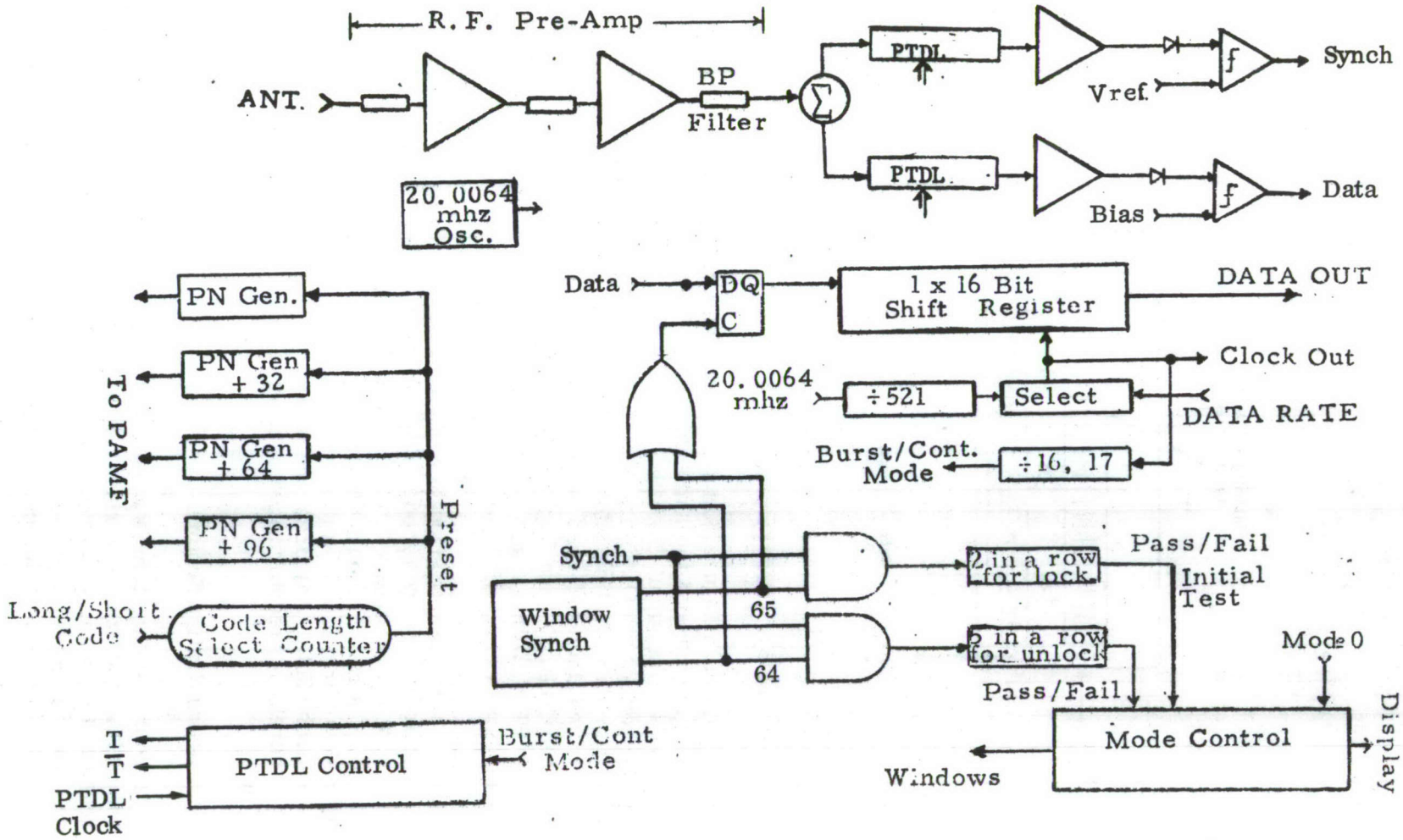


Figure 50. PTDL Interface Transceiver (Receiver)

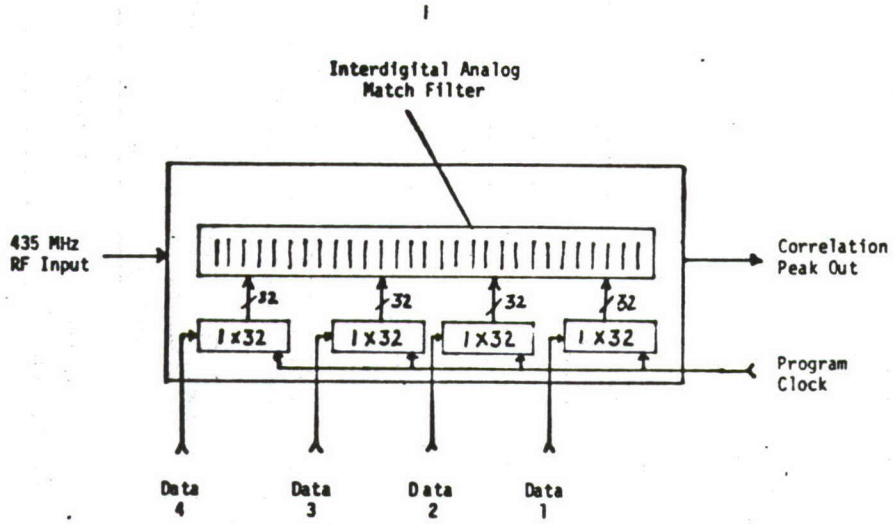


Figure 51. Programmable Tapped Delay Line

The receiver shown in Figure 50 used two PTDL's programmed Q, $\overline{Q}$, and Q, Q. Both lines are loaded with the same data for the first 64 chips and with opposite data for the second 64. An output from the Q, $\overline{Q}$ PTDL would signify a digital "1" and correspondingly out of the Q, Q, a "0". Data then is summed together after video detecting for synchronization information and their difference is examined for data information. Two lines are used so that maximum processing gain benefits may be obtained from the PTDL. Four separate PN generators (each staggered by 32 clocks) load the PTDL with a starting vector after which the generators are themselves advanced 32 clocks so as to be ready to load the next vector.

The receiver operations are tied to a mode control (Figure 52). The operation just described is called the search mode (M3). After a correlation occurs the PTDL's are loaded with a new vector and their outputs blanked until a specific predictable window time frame occurs. The outputs are then enabled (M5) 64 and 65 clock periods later and examined for presence of any correlation peaks. Any absence returns the system back to search (M3). Any presence places the system into a data lock cycle (M6, M7, M8), whereby a predetermined number of failures (30) returns the receiver back into search.

Receiver Synchronization Scheme

The time frame of the system is such that it is completely synchronous to the system reference (20.72 MHz). The receiver clock is set to operate at 20.72 MHz whereas the transmitter is set to operate at a slightly lower frequency of 20.719 MHz. In this manner, any correction made in a digital tracking loop can be made in one known direction. After detecting a starting correlation vector the PTDL outputs are blanked

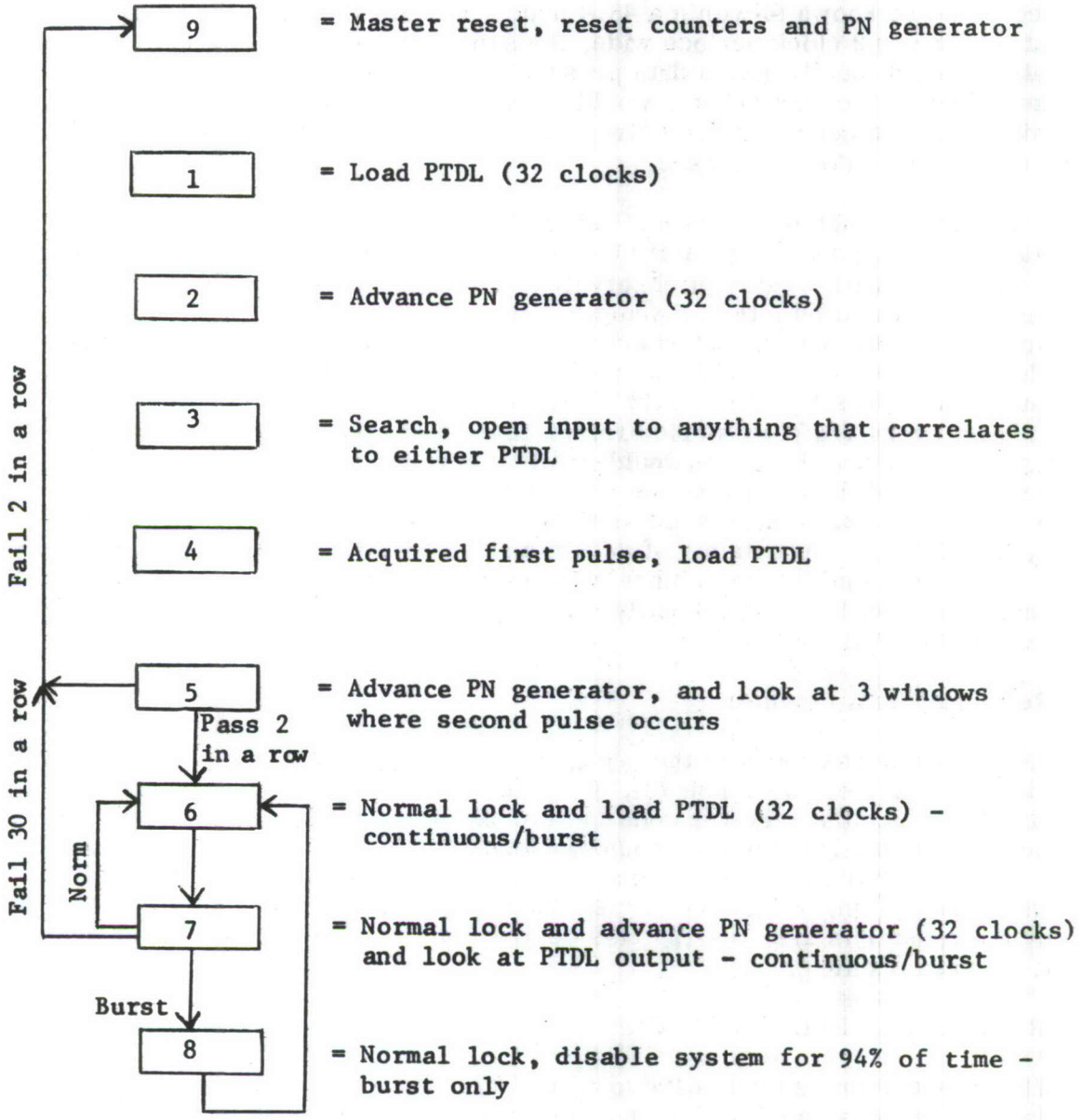


Figure 52. Receiver Operating Sequence

until 64 and 65 clock periods later. Any correlation peak detected in the 65th window would be an indication that the receiver clock is running too fast and should be blanked one clock period. This would place the next correlation peak 64 receiver clock periods away at the higher clock rate. (This also is the correlation peak separation.)

Clock synchronization would be derived by disabling one clock period to the system whenever correlation presence would be found in the 65th window. Data presence would be known to within a 48.4 nsec uncertainty. Since the base of the correlation peak is 2 clock periods wide, the sum of the auto correlation with its anti-correlation should ideally give a data presence of 96.5 nsec. Consequently, the 48.4 nsec clock correction scheme would be more than adequate to handle the incoming data which would be edge sampled between the 64th and 65th clock. This would give an uncertainty region of ±24.1 nsec.

One evident problem in this method of clock tracking is the system's susceptability to noise making a full clock correction rather than the correlation peak. i.e. If during the 64th window of observation, noise would trigger the threshold detector, the observation interval would be closed during the 65th window where the true correlation peak occurs and where a clock correction is required. This would cause the system to drift out of lock in a high noise prevalent environment. System loop bandwidth is presently 20.7 MHz. Consequently, clock corrections should be made at least every 1/4 clock period rather than a full clock period. In the digital tracking loop described above this would entail running the receiver from a 82.88 MHz clock reference and then blanking one of these clock periods rather than a 20.72 MHz clock period. The 82.88 MHz could then be divided down to provide the rest of the system, 20.72 MHz. Uncertainty of data sampling would be reduced from ±24.1 nsec down to ±6.03 nsec and the probability of noise occurring prior to a correlation in the 64th window has now been significantly reduced (loop bandwidth has also effectively been reduced to 5 MHz).

Redundant Data Detector

A subsystem was added to the receiver which takes advantage of the redundantly encoded data bits, i.e., 19.2 kbit (0), 9.6 kbit (1), 4.8 kbit (3), 2.4 kbit (7), and 1.2 kbit (15). Since the receiver code is synchronous to the transmitter and data transitions are known, an up down counter clocked at 19.2 kHz serves as an ideal decision device. A digital word comparator senses the counter output level at a given baud rate of reception; and a decision is made at the start of each new transition whereby the counter is also reset. This device demonstrated a net improvement in B.E.R. of up to 5×10^{-2}.

4.3 TRANSCEIVER PERFORMANCE

The transceiver was delivered to ECOM 27 February 1975 and satisfactory operation was demonstrated during acceptance tests. At low data rates (1.2, 2.4, and 4.8 kbit) an acceptable error probability (P_c) of 10^{-2} to 10^{-4} was experienced. Long code(2.23) acquisition times amounted to a rapid 7 - 16 seconds while in the burst reception mode. Receiver minimum sensitivity was recorded to be -90 dBm. System sensitivity was designed to be -100 dBm. However, due to additional unpredictable insertion loss (55 dB) found in the PTDLs, it was necessary to use some of the modular amplifiers found in the front end as post PTDL amplifiers. This dropped the front end sensitivity down -10 dB to -90 dBm, (front end N.F. was measured to still

be <5 dB). It is therefore recommended that the amplifiers removed from the front end be replaced. It was noted that front end sensitivity could be heightened by 10 dB by making the thresholds on the threshold detectors adaptive; i. e., when the receiver goes into data lock, the analog thresholds could be dropped to a predetermined level, allowing a data unlock of -100 dBm, i. e., -90 dBm MDS and -100 dBm dropout.

The performance of the receiver is illustrated in Figure 53. The measured peak to sidelobe for the delay lines was 15 - 16 dB for an optimum 127 chip PN sequence under ideal conditions. (Theoretical is 23 dB.) Excessive noise in the receiver reduced this 15 dB peak to sidelobe ratio down to a lower ratio. This was due to the high speed noise prevalent in the Schottky devices used to achieve complete synchronism to the 21 MHz reference. As a consequence, the average peak to sidelobes was reduced by several dB to 11 - 12 dB. Consequently, the system input thresholds had to be set lower, closer to the noise, making the system more vulnerable to coherent noise such as jamming. The peak to sidelobe ratio shown in Figure 54 appears to be 8 dB; however, one must remember that the correlation peaks are sample gated and the noise seen between correlation peaks represents the programming of the PTDL's. The noise seen during non-burst is somewhat representative of the sidelobe quantity thus giving an effective 11 dB peak to sidelobe ratio.

Dissimilar amplitudes (±3 dB) noted in the video detected sum outputs Figure 55 are due to individual tap irregularities. The first delay lines used in the development of the transceiver had 15 taps that were nonprogrammable. Consequently, depending on the code, a variable number of tap outputs add coherently to produce correlation peaks with the noted amplitude variations.

Another reason for the amplitude variations is the irregular transmission line loss effects in the control IC's within the PTDL which are also code tap dependent. Uniform tap outputs with low phase errors could be achieved by suitably adjusting tap apodization and position to compensate for the amplitude dissimilarities.

The main purpose of the program was successfully accomplished. This was to demonstrate the programmable acoustic signal processing devices could be used to demodulate 20. 7 mcps spread spectrum waveforms directly from a UHF 435 MHz carrier.

Significant reduction in hardware has been realized with the use of these PTDLs in the receiver. In addition, processing gains can be utilized fully whereas in digital matched filters quantization losses reduced any potential benefits derived from multitap summation networks. It has been demonstrated that a completely new and viable range of signal conditioning formats has been made available to the system designer with these VHF programmable tapped delay lines.

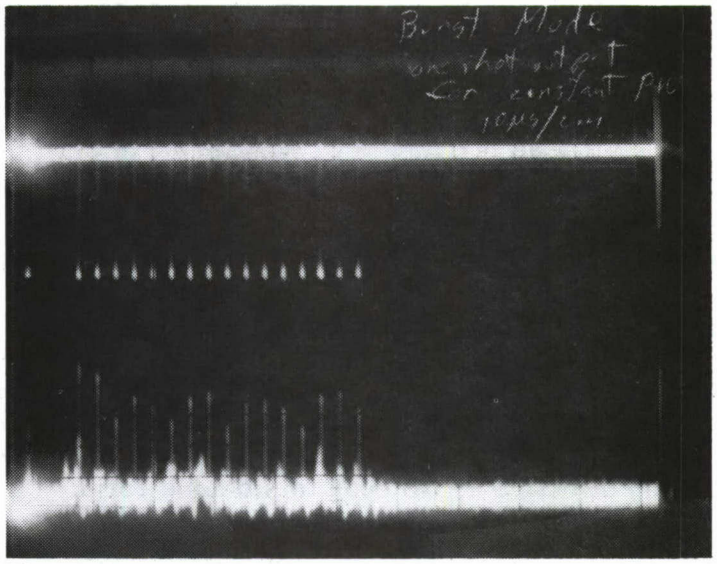


Figure 53. Burst Mode (10 μsec/cm)

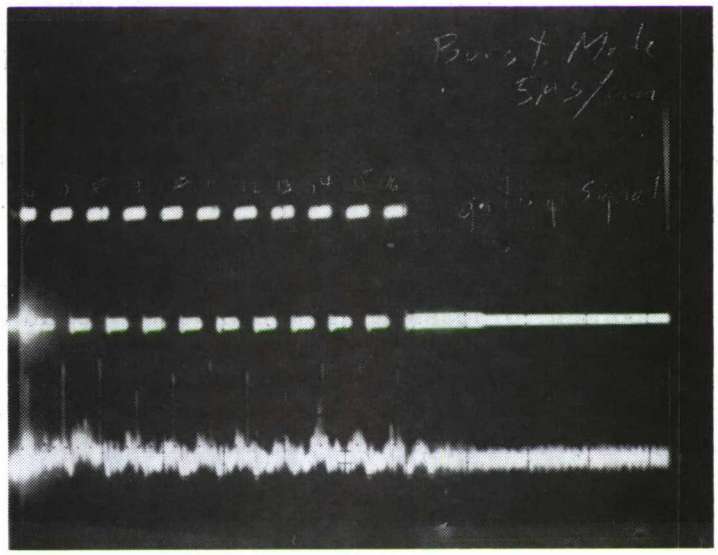


Figure 54. Burst Mode (5μsec/Division)

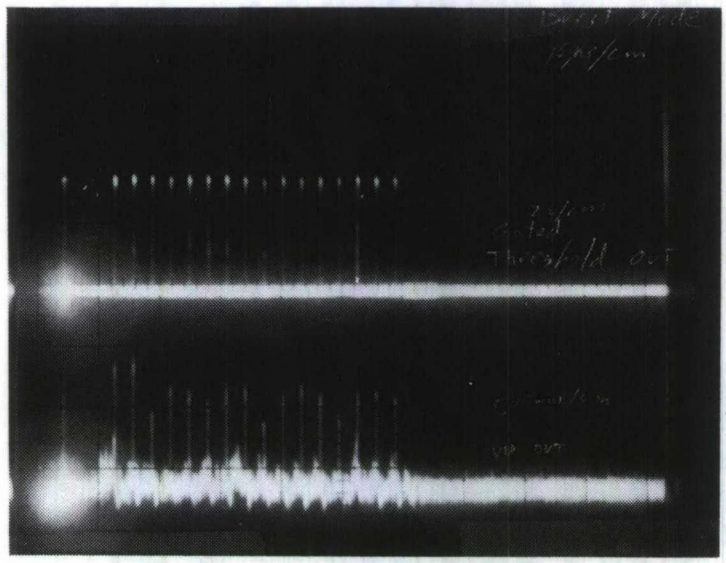


Figure 55. Burst Mode (15 μsec/Division)

5. CONCLUSIONS AND RECOMMENDATIONS

Based on the theoretical and experimental work carried out on this contract the following main conclusions can be drawn:

1. Electronically programmable 128 tap acoustic matched filters for spread spectrum biphase modulation and demodulation of a 435 MHz carrier at chip rates of 20.7 MHz are practical, and the use of these devices in a UHF transceiver delivered to ECOM has been successfully demonstrated.

2. Matched filter performance at 435 MHz requires further improvement before the excellent device performance acheived at VHF (70 MHz) on other programs can be matched at UHF. The special problems encountered on this program at UHF frequencies are associated with lossy transmission line effects in the integrated circuits used to control the acoustic taps. These effects were identified, quantified, and correlated satisfactorily with experimental results during the course of this program. The quantitative data generated will allow these effects to be compensated for in subsequent UHF device designs.

3. Serial input digital programming data rates of 50 MHz can be acheived with the CMOS on sapphire integrated control circuits developed on this program. Each integrated circuit controls 16 acoustic taps, eight integrated circuits are therefore required for each 128 tap acoustic line. To reduce code loading time each of the eight ICs could be accessed simultaneously in parallel with a 16 chip subset of the 128 chip code to give a loading time equal to 16 times the 20 nsec clock period, or 320 nsec. A further ~ 30 nsec would be required to transfer the data to the holding register and lock out the input register, so a minimum code load time of 350 nsec is possible.

4. Sufficient experience has been obtained with the CMOS/SOS integrated control circuits developed on this program to demonstrate a yield in excess of 20 percent should be acheivable in production.

5. Active versus passive waveform generation techniques were examined as a subtask on this program and information was generated for the specific waveform of interest to this contract (435 MHz carrier, 20.7 MHz chip rate, 127 chips) which can assist a systems engineer in deciding which approach would be best for a particular system.

The feasibility of useful VHF electronically programmable surface wave matched filters for spread spectrum waveforms has been demonstrated on this contract. Further development work is recommended to significantly improve UHF device and transceiver performance. This work, in the device area, would be directed towards reducing the effects of transmission line loading in the ICs to negligible levels by a combination of integrated circuit modifications and suitable compensation techniques based on the data obtained on the current program.

Additional recommended work on the UHF transceiver includes redesigning to include an 80 MHz reference and the use of a quarter clock correction rather than the present full clock correction scheme of data and clock lock. B.E.R. will be improved

by a factor of 100 by this measure. A redesign is recommended to accomodate a variable or adaptive minimum sensitivity data lock threshold, and then drop out at a lower more sensitive threshold, e.g. -100 dBm "data lock" and "acquire", -110 dBm "data unlock" and search.

6. REFERENCES

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